IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; CHI, MEI OPTOELECTRONICS CORPORATION; and CHI MEI OPTOELECTRONICS USA, INC., Defendants.	C.A. No. 06-726-JJF **CONSOLIDATED CASES**
AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG DISPLAY AMERICA, INC., Defendants.	C.A. No. 07-357-JJF

AUO'S RESPONSIVE CLAIM CONSTRUCTION BRIEF FOR LG DISPLAY'S PATENTS

OF COUNSEL:

Vincent K. Yip
Peter J. Wied
Terry D. Garnett
PAUL HASTINGS JANOFSKY & WALKER LLP
515 S. Flower Street, 25th Floor
Los Angeles, CA 90071

Ron E. Shulman
Julie M. Holloway
WILSON SONSINI GOODRICH & ROSATI
650 Page Mill Road
Palo Alto, CA 94304

M. Craig Tyler
Brian D. Range
WILSON SONSINI GOODRICH & ROSATI
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, TX 78759

Richard H. Morse (#531)
John W. Shaw (#3362)
Karen L. Pascale (#2903)
Andrew A. Lundgren (#4429)
YOUNG CONAWAY STARGATT & TAYLOR LLP
The Brandywine Bldg., 17th Floor
1000 West Street
Wilmington, DE 19801
(302) 571-6600

Attorneys for AU Optronics Corporation and AU Optronics Corporation America

September 4, 2008

TABLE OF ABBREVIATIONS

'274 Patent	U.S. Patent No. 5,905,274
'321 Patent	U.S. Patent No. 6,815,321
'374 Patent	U.S. Patent No. 7,218,374
'449 Patent	U.S. Patent No. 5,825,449
'489 Patent	U.S. Patent No. 7,176,489
'569 Patent	U.S. Patent No. 6,664,569
'737 Patent	U.S. Patent No. 4,624,737
'984 Patent	U.S. Patent No. 6,803,984
AUO	AU Optronics Corporation and AU Optronics Corporation America
Chen Decl.	Declaration of Hua Chen in Support of AUO's Opening Claim Construction Brief [D.I. 380]
Second Chen Decl.	Second Declaration of Hua Chen in Support of AUO's Responsive Claim Construction Brief [D.I. ___] (filed contemporaneously herewith)
Ex.	Exhibit
Fig.	Figure
Holloway Decl.	Declaration of Julie M. Holloway in Support of AUO's Opening Claim Construction Brief [D.I. 382] (filed in paper format)
JCC	Joint Claim Construction Chart [D.I. 376]
Joint Ex.	Joint Submission of Patents and Prosecution Histories (to be filed by the parties)
LGD	LG Display Co., Ltd. and LG Display America, Inc.
CMO	Chi Mei Optoelectronics Corp. and Chi Mei Optoelectronics USA, Inc.
AUO Brief	AUO's Opening Claim Construction Brief [D.I. 378]
LGD Brief	Opening Claim Construction Brief of Plaintiff LG Display Co., Ltd. [D.I. 384]
CMO Brief	Memorandum in Support of Defendants Chi Mei Optoelectronics' Proposed Claim Constructions [D.I. 383]

NOTES:

- Emphasis added throughout, unless otherwise noted. In general, internal citations and quotations are omitted.
- A revised version of Appendix A is attached to this brief. (This version corrects some typographical errors in the version submitted with AUO's Opening Claim Construction Brief.) This is submitted solely for the Court's convenience; the Joint Claim Construction Chart [D.I. 376] is the controlling authority on the parties' positions.

TABLE OF CONTENTS

TABLE OF CONTENTS
(continued)

TABLE OF CONTENTS
(continued)

TABLE OF AUTHORITIES

Page(s)

CASES

I. INTRODUCTION

While contending, on one hand, that the Court should adopt the majority of the constructions from the previous litigation (whether set forth by the Court or agreed to by parties that did not include the current Defendants), LGD selectively disputes several of the previous Court's constructions, unremarkably on claim terms on which the Court had already ruled against LGD. LGD should not be allowed to reargue the same rejected constructions. While it is true that certain constructions need clarification, it is not for the reasons set forth by LGD, but rather because those constructions are either based on fundamentally flawed agreements previously made by LGD and CPT or should be further explained to reduce ambiguity and prevent unnecessary future disputes. For the reasons set forth herein, AUO respectfully requests that the Court adopt its proposed constructions.[1]

II. LGD'S ASSERTED PATENTS

A. Common Terms

AUO submits that these terms must be construed consistently: consistently between patents and consistent with other claim constructions. LGD has not, and cannot, show that some of its patents adopt different definitions for these common, industry terms, and thus they should be given one construction for the purposes of all patents.

---

[1] Regrettably, the parties have been unable to agree on the application of Local Rule 7.1.3(a)(4) in this unique context – a multi-party consolidated action involving 23 patents, in which each party is both asserting and defending infringement claims. LGD has been adamant that it is entitled to file and intends to file two 40-page briefs. Whatever the proper construction of Local Rule 7.1.3(a)(4) might be in this circumstance, AUO respectfully submits that it cannot possibly provide that LGD is entitled to twice as many pages as AUO for its responsive Markman briefing. The Court's Oral Order of August 26, 2008 did not imply otherwise. Like LGD, AUO must respond to the separate arguments of two parties - LGD and CMO - regarding two separate sets of patents. Therefore, AUO is likewise filing two separate briefs of no more than 40 pages each.

1. "thin-film transistor" ('737 Patent) / "thin film transistor" ('449 Patent) / "transistor" ('274, '321, '489 Patents)

AUO's proposed construction would treat this term consistently across the patents, while LGD, inexplicably, offers a slightly different construction for the '274 Patent versus the '321 and '489 Patents. This is particularly surprising since the three patents all share the same disclosure; thus, the '274 Patent could not have adopted a construction different from the other patents.

Likewise, AUO's proposed construction is consistent with the construction of other terms by recognizing that the current in a transistor flows between a source electrode and a drain electrode. While LGD refers simply to "terminals" in its construction of transistor (e.g., Claim 1 of '737 Patent), its construction of "gate electrode" in the same claim recognizes that the "terminals" between which the current flows are the source and drain electrodes. Appx. A at pp. 1-2. Rather than using different words in different constructions, which could introduce confusion and ambiguity, AUO submits that the Court should adopt its construction so that the construed terms uniformly and consistently refer to the source, drain and gate electrodes of a transistor.

Likewise, although it is unclear whether LGD seriously intends to argue that a thin film transistor is not a semiconductor device, LGD nonetheless removes that phrase from its proposed construction of the '449 Patent (but retains it for '274 and '321 Patents). AUO's proposed construction eliminates this unexplained deviation from the commonly-understood meaning of the term.

2. "gate electrode" ('737, '449, '569 Patents) / "gate" ('274, '321, '489 Patents)

Once again, AUO seeks constructions that are consistent not only between patents but with other terms in the same patent. The terms "source electrode" and "drain electrode" were previously construed by another court, and the parties have largely agreed with those

constructions.[2] Those constructions indicate that the source and drain electrodes are formed in the source and drain regions, respectively. AUO therefore seeks a consistent construction that indicates the gate electrode is formed in the gate region.

3. "XXX formed on YYY" ('449 Patent, claims 1 and 11) or "forming XXX on YYY..." ('321 Patent, claims 7 and 16;'737 Patent, claim 1;'002 Patent, claim 1)

This presents another term which, though used in a consistent manner by several of the patents, is construed differently by LGD for different patents. LGD agrees that "forming/formed on" in the claims of the '449 and '321 patents require the layer formed to be "above ***and*** in contact" with the surface on which it is formed (*See* JCC, Ex. C, p. 2-5 and Ex. G, p. 2), but it changes its position for the '737 and '002 patents, requiring only that the layer be "above and supported by ***or*** in contact with" the surface on which it is formed. This is inconsistent with the specific claim language at dispute here for the '737 and '002 patents, which call for forming one layer/pattern above and in contact with the layer/pattern below it. *See* '737 Patent, Claim 1; '002 Patent, Claim 1. The specifications also show that these patents use the term consistent with the other patents to mean a layer is above and in contact with another layer. *See* '737 Patent at Figs. 2-3, 2:8-16, 3:23-28; *see also* '002 Patent at 5:24-32, 5:2-6, Figs. 3 (ITO 46 on the left in the area of pixel pad 68) and 6 (pixel 166).

LGD attempts to support its position by ignoring the larger terms "forming on" and "formed on", and focusing solely on the word "on". This is contrary to the requirement to look at the surrounding claim language and construe terms in context. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005). Moreover, LGD's argument is based on the use of the word "on" in the phrase "depositing on" and is therefore irrelevant to the proper construction of

[2] The only difference is that CMO proposes they be construed as a single term, while AUO and LGD propose separate constructions of the terms.

"forming/formed on". One understands that the word "on" can have different meanings when used in different phrases; for example, one understands that it means something different to talk ***on*** a phone than to sit ***on*** a chair. Thus, even if LGD were right that "depositing on" cannot require direct contact, it does not follow that "forming on" cannot require direct contact. Because the language of the claims and specification of the '737 and '002 Patents points to these terms having the same meaning as in the other patents, AUO respectfully requests that the Court adopt its proposed constructions for all of the patents.

B. '737 Patent

The opening briefs dispute AUO's proposed construction for several groups of limitations: (1) "without exposing them to an oxidizing atmosphere"/"oxidizing atmosphere;" (3) said source and drain electrode serving as at least a part of the mask"/ "serving as at least part of a mask"/ "mask;" and (4) "continuously depositing"/"depositing."[3]

1. "without exposing them to an oxidizing atmosphere"/"oxidizing atmosphere" (claim 1)

The primary dispute between LGD and AUO's construction is whether this limitation allows exposure to small amounts of oxidizing agent that may create an un-detectable amount of oxidation.[4] To be consistent with the '737 Patent specification, AUO contends that the atmosphere in question must not have an oxidizing agent and, thus, LGD's construction is too broad because it permits some oxidation. To support its proposed construction, LGD puts forth the unsubstantiated assertion that one of ordinary skill in the art would understand that "small or insignificant amounts of oxidizing agents, or an atmosphere that would not impair the electrical

---

[3] Another set of limitations relating to "forming … on" is discussed above.

[4] AUO's proposal for "oxidizing atmosphere" is "atmosphere containing oxidizing agent." LGD's proposal is "an atmosphere that would create a detectable amount of oxidation on a film." JCC, Ex. A.

characteristics of a thin film transistor, would not be an 'oxidizing atmosphere.'" LGD Brief, 13. Surprisingly, this statement is not supported by an expert declaration, inventor's testimony, dictionaries, or learned treatises. Nor is it supported by the intrinsic record. *See* LGD Brief, 13.

LGD's position is further misplaced because the meaning of this limitation could be easily ascertained by its plain meaning and the intrinsic evidence. The intrinsic record for the '737 Patent is clear – no exposure to any oxidizing agent. *See* '737 Patent, Abstract ("without exposing them to *any* oxidizing atmosphere."); 3:53-55 (no oxides are formed). *See Phillips*, 415 F.3d at 1317 ("However, while extrinsic evidence can shed useful light on the relevant art, we have explained that it is less significant than the intrinsic record in determining the legally operative meaning of claim language."). Indeed, the text surrounding LGE's citation to the '737 Patent specification (1:41-44) actually supports AUO's proposed construction. In discussing the prior art, the specification explains that removal of an oxidation film with acid still results in impairment of electrical resistance because some oxygen and impurities remain on the surface. *See* '737 Patent, 1:32-46. Thus, the patent specification makes clear that the invention utilizes an oxidizing agent free environment so that no oxidation occurs during manufacture of a thin film transistor.

2. "Said source and drain electrode serving as at least a part of the mask"/ "Serving as at least a part of the mask"/"mask" (claim 1)

The key dispute for this group of limitations is the proper construction of the term "mask." Provided below is a side-by-side comparison of each party's proposal.

AUO	LGD	CMO
a pattern to define the boundary for the removal or formation process	a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed	a top surface pattern above one or more layers of material that will be selectively removed according to the shape of the mask. The mask is made of material that is resistive to the removal technique and defines by its edges the boundaries of the material selected for removal

It is apparent that all parties agree that a "mask" is a pattern that is utilized in a mask/etching process. AUO's proposal clarifies the role of a mask as a pattern that defines the boundaries for removal; LGD's proposal stresses that the pattern must be made of material that is resistive to the removal technique, but vague as to how this pattern affects the selective removal process; CMO's proposal offers an alternative that requires a mask to define boundaries, and to be resistive to removal.

a. AUO's proposed construction captures the essential role of a mask

There is little dispute among the parties as to how a mask/etching process works as part of the fabrication process for a semiconductor device. For example, LGD describes in its Markman brief submitted to the California Court the masking process working as follows: forming a mask with a designed pattern above the surface of the material that needs to be patterned (e.g., a thin film of silicon), removing part of the surface of the material that is exposed by a removing technique (e.g., etching away the exposed surface), and consequently forming a pattern matching the mask in the surface of the thin film at the end of the process. Second Chen Decl., Ex. 1, LG. Philips LCD Co., Ltd.'s Opening Claim Construction Brief, pp. 46-47. The treatise cited by CMO notes that masks contain patterns of windows that are transferred eventually to the surface of the silicon wafer. CMO Brief, p. 9. The specification of the '737 Patent teaches that the source and drain electrodes serve as at least a part of the mask because they shield the portions of the conductive film underneath them from removal. *E.g.*, '737 Patent, Fig. 2d and 2:60-66. It is undisputed, therefore, that what is removed from, or what remains on, the surface is defined by the mask configurations. Because the goal of a mask/etching step is to

form a pattern on (or transfer to) a surface, the mask must define boundaries of removal. AUO's construction captures this essential role.[5]

LGD's proposal, on the other hand, disregards this role because it does not specify the relationship between the pattern of a mask and the boundaries of removal. According to LGD's proposal, a mask needs only to be "a pattern above a surface from which material is to be selectively removed." LGD's construction does not recognize any relationship between the shape of the mask and the shape of the pattern formed on the surface, and is therefore wrong.

b. Plaintiff's proposal leads to the unreasonable possibility that source and drain electrodes would constitute part or all of a mask[6] yet have no impact on the boundaries of removal

Applying LGD and AUO's proposed constructions to the following scenario results in different outcomes. Suppose that there are two layers of material on top of a thin film surface – an upper layer (photoresist layer) with one pattern, and a middle layer (metal layer) having a nearly identical or slightly smaller pattern viewed from above, both being resistive to the removal technique. Assume further, there is no point in time during the etching process that part of the upper layer is completely etched away, so that the middle layer is never exposed to etching and is not needed to provide added shielding of the thin film surface area to create the desired pattern. Under AUO's construction, the middle layer is not part of the mask because it plays no role in defining the boundaries of removal. Under LGD's construction, however, the middle layer could be viewed as part of the mask because it is part of "the pattern above a surface from

---

[5] It follows, therefore, the longer limitation of "said source and drain electrode serving as at least a part of the mask" should be construed to require that the source and drain electrode be able to at least partially define the boundaries of removal.

[6] The limitation recites "said source and drain electrode serving as at least a part of the mask." Its plain meaning suggests that the limitation reads not only on scenarios where the electrodes serve as part of the mask, but also on scenarios where the electrodes serve as the mask.

which material is to be selectively removed," and it is "made of material that is resistive to the removal technique." Because the middle layer exerts no influence on the boundaries of removal or the pattern ultimately created in the thin film surface, such an outcome resulting from LGD's construction contradicts the common understanding of a mask's role. LGD's construction therefore cannot be right.

c. Plaintiff's proposal improperly conflates the two distinctively claimed steps

Claim 1 of the '737 Patent recites two distinct steps: a fourth step for "selectively forming a source and drain electrode … [that are] spaced apart from each other," and a fifth step for "selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask." AUO's proposal requires that the electrodes have a role in defining the boundaries of removal, therefore underscoring that step four and step five are separate and distinct. LGD's proposal, on the other hand, ignores this distinction and is inconsistent with the surrounding language of the claim.

3. "Continuously Depositing"/"Depositing" (claim 1)

The dispute relating to this group of limitations centers on whether depositing means just "forming" or more specifically "precipitating."[7] AUO submits that its construction is supported by the plain meaning of the term "deposit." AUO Brief, 31. Furthermore, claim 1 of the '737 Patent recites in multiple places the verb "forming," e.g., "the first step for forming a gate electrode …", '737 Patent, 4:26-28; "a fourth step for forming a source electrode and a drain electrode …," '737 Patent, 4:36-38. Claim 1 also recites the verb "deposit" in a number of places, e.g., "a second step for continuously depositing …." '737 Patent, 4:27-29; "a sixth step

[7] AUO withdrew the proposed construction of "chemically precipitating" before filing its opening brief.

for depositing ….", '737 Patent, 4: 42-43. Two distinct terms should not be construed to be the same. *See Bancorp Services, L.L.C. v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1373 (Fed. Cir. 2004) ("the use of [two] terms in close proximity in the same claim gives rise to an inference that a different meaning should be assigned to each.").

C. '002 Patent

1. Claim terms LGD failed to address in its opening brief

LGD does not address several disputed terms in its opening claim construction brief.[8] LGD instead relies on its JCC chart. *See* LGD Brief, pp. 1-2. However, the purported "support" cited by LGD in its portion of the JCC chart is either insufficient or irrelevant, and its proposed constructions are either unclear or simply read out limitations altogether. Thus, AUO respectfully requests that the Court adopt the proposed constructions set forth in AUO Brief and JCC chart.

2. "interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another" and "interconnecting" and "substantially all" (claim 1)

By its construction, LGD hopes to completely undo the Court's previous construction of "interconnecting," read away the word "substantially," and twist the meaning of "interconnecting…to one another." LGD's misguided efforts result in a proposed construction that lacks clarity and deviates from the plain meaning. LGD further disregards the consistent use of the claim term within the '002 Patent, which this Court recognized in the previous litigation,

---

[8] The claim terms LGD failed to address for the '002 Patent include "forming a plurality of row and column intersecting pixel activation lines" (claim 1), "to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the display" and "protection from electrostatic discharges" and "row and column activation lines" (claim 1), and "inner electrostatic discharge guard ring" (claim 8).

and attempts without any basis to broaden the scope of the term beyond how it was consistently used and described.

Rather than looking at interconnecting the plurality of "row/column lines to one another," LGD seeks to introduce confusion by asking this Court to look at a portion of the term "to one another" out of context. Curiously, rather than discussing how the specification and the claim describe the manner in which these plurality of row/column lines are to be connected to each other, LGD points to connections between irrelevant structures such as the outer and inner guard rings and their uses, and the connections between two redundant row/column lines of a sub-pixel. *See* LGD Brief, p. 9; *see also* '002 Patent, Fig. 4. On the other hand, AUO's proposed construction of "joining almost all of the row lines to one another and joining almost all of the column lines together" is entirely consistent with the patent's teachings as this Court previously recognized. *See* Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 6; *see also* '002 Patent, 8:5-8 and '222 Patent,[9] 6:51-55 ("row (gate) lines or buses" are joined together "by respective lines or shorts 158, 160…170"), 6:61-65 ("column (source) lines or buses" are joined together "by respective lines or shorts 192, 194…204"), 7:39-55 ("row bus lines 18 are interconnected…by a plurality of connecting lines… In a like manner, the column bus lines are interconnected…by a plurality of connecting lines.").

With respect to the term "interconnecting," while AUO believes that the word "joining" here would better serve to clarify the meaning of "interconnecting," LGD seeks to reargue a construction that it lost in the last litigation. Here, LGD proposed "electrically connecting with ***conductive material*** (emphasis added)." JCC, Ex. B, p. 3. LGD's opening brief makes clear that it hopes to include the use of connecting by "semiconductor" material within the scope of this

---

[9] AUO Brief, p. 35. *See* Chen Decl., Ex. 2. U.S. Patent No. 4,820,222.

claim term. *See* LGD Brief, p. 8. LGD's proposed construction, however, does nothing but introduce ambiguity, by arguably allowing a "***semi***conductor" to be considered "conductive material" (which ignores the fundamental difference between a conductor and a semiconductor).

Moreover, if LGD is to have its way, the Court's previous construction and reasoning would be completely eviscerated,[10] and the claim rewritten to a scope far beyond the teachings of the '002 Patent. Here, the relevant interconnection is the interconnection of the "said [plurality of] row lines" and the interconnection of the "said [plurality of] column lines," not just any connection. The '002 Patent and its incorporated '222 Patent clearly teach that a set of jumpers/lines/shorts are used to join the row lines together and another set of jumpers/lines/shorts being used to join the column lines together. *See, e.g.*, '002 Patent, 8:5-8; *see also*, '222 Patent, Figs. 6 and 7, 6:51-55, 6:61-65 7:39-55. LGD's use of "conductive material" ignores these teachings entirely. Finally, using "joining" here, as AUO proposes, would clarify the ambiguity and inconsistency that LGD seeks to ***reintroduce***. The Court should adopt AUO's proposed construction of "joining almost all of the row lines together and joining almost all of the column lines together" for the entire limitation, as it is consistent with the plain meaning of the phrase and the teachings of the patent. *See* JCC, Ex. B, pp. 3-4.

3. "outer electrostatic discharge guard ring" (claim 1)

The outer electrostatic discharge ("ESD") guard ring is not, as LGD and the previous defendant CPT proposed, "a closed or open ring, or open L or C-shaped line." In the previous litigation, the Court merely accepted this interpretation because the then defendant CPT agreed to it. AUO Brief, p. 36. A close reading of the specification reveals that this proposed

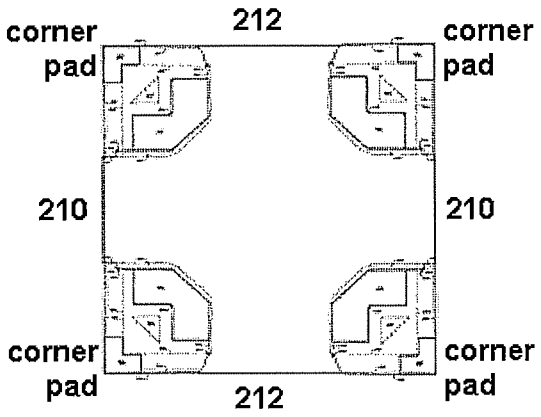
---

[10] This Court recognizes that "'[i]nterconnecting' is consistently described or illustrated in figures as using 'lines', 'shorts', or 'jumpers', i.e., conductors, to connect electrical elements." *See* Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 6.

construction errs by associating an open L or C-shaped line for the *inner* guard line with the outer guard ring. Moreover, this open L or C-shaped line is created only under a specific condition for the *inner* guard line when and "***if*** the gate and source pads all are on one respective side of the display (emphasis added)." *See* AUO Brief, pp. 36-37; *see also* '002 Patent at 7:19-21. The description of the outer ESD guard ring, along with the drawings, in the '002 Patent clearly shows that the outer ESD guard ring is a surrounding structure:

8

The ESD preventive structure can also include an outer ESD guard ring **200**, best illustrated in FIG. 7. Only one corner portion **202** of the display and guard ring **200** is illustrated. While the display is being manufactured, the outer guard ring **200** is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines **204** and **206**. A corner pad **208** is connected to each other corner pad (not illustrated) by respective outer conductive lines **210** and **212** of the guard ring **200**. The L-shaped corner pad **208** can be



See '002 Patent at 8:3-4, 8:8-11. Therefore, this limitation should be construed as "a surrounding structure outside the active matrix display to provide protection from electrostatic discharges." JCC, Ex. B, p. 7.

4. "resistance" (claim 1)

LGD misses the point by characterizing the dispute here as a "resistance" vs. "resistor." In actuality, LGD seeks to do away with the "specified" value of resistance this Court incorporated into the prior construction (based on the clear teaching of the '002 Patent). *See* Chen Ex. 3, Judge Farnan Memorandum Order, pp. 12-13. Provided below is a side-by-side comparison of the Court's previous construction, and AUO's and LGD's proposed constructions:

The Court's Prior Construction	AUO's Proposed Construction	LGD's New Proposed Construction
A circuit component that has a ***specified*** resistance to the flow of electric current and is used to minimize the current surge from electrostatic discharge	A circuit component that has a ***specified*** ratio between voltage and the flow of electric current, and is used to minimize the current surge from electrostatic discharge[11]	a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge

The construction LGD asks the Court to adopt in this case is similar to the construction LGD had proposed in the previous litigation, in hopes that it might later argue "[a]ll circuit components…have the characteristics of resistance [as understood by LGD]."[12] *Id.* at p. 10. Much like how LGD erroneously seeks to turn a "conductor" into a "semiconductor" in the previous claim term "interconnecting…," LGD hopes to similarly broaden and rewrite the claim term "resistance" so that LGD might later argue that "[a]ll circuit components" are covered. LGD's proposed construction defies sound claim construction principles, ignores the intrinsic evidence and is at odds with this Court's previous ruling.

As the Court determined before, the only guidance as to the meaning of this term is the single embodiment in which it appears. *Id.* at p. 12; *see also* '002 Patent at 8:1-39. Here, this "resistance" is not just any resistance, but "a ***large*** resistance 228, such as 100 K ohms (illustrated schematically)" (emphasis added). *See* '002 Patent at 8:25-26. The value of the resistance is specified as large, and an exemplary specified value of 100 K ohms is even given.

---

[11] Under AUO's proposed construction, instead of using the term "resistance" again in the construction for "resistance," the terms is replaced with its ordinary meaning from the IEEE Standard Dictionary of Electrical and Electronics Terms.

[12] As the Court noted in the previous litigation, "LPL contends that because '[a]ll circuit components…have the characteristic of resistance,' the Court should construe 'resistance' as 'any component used to caused a voltage drop during current flow.'" *See* Chen Ex. 3, Judge Farnan Memorandum Order, p.10.

The teaching of the patent and this Court's recognition of the "specified" resistance is crystal clear.

While LGD seeks to discard the word "specified," AUO's proposal keeps it and further provides clarity by replacing the term "resistance" from the Court's previous construction with its plain, ***technical*** meaning, which specifically recognizes the relationship between voltage and current. *See* AUO Brief, pp. 37-38 and fn. 18-19. The Court should, therefore, adopt AUO's proposed construction, which is consistent with the Court's prior construction and clarifies any ambiguity.

5. "removing said outer guard ring and row and column interconnections" and "removing" (claim 1)

While AUO contends that this entire limitation is indefinite in its opening brief, LGD's position rests solely on an erroneous agreement between LGD and previous defendant CPT. An indefinite term does not become definite simply because CPT failed to raise the defect in the previous litigation. In the context of the claims and specification, the patent fails to clearly teach the removing step, so its meaning (and the scope of the claims) cannot be determined. *See* AUO Brief, pp. 39-40; *see also* CMO Brief, p. 17.

In the event the Court is inclined to construe this limitation, AUO respectfully contends it should be construed as "physically disconnecting (and removal of) said guard ring and lines connecting/joining the row and column, intersecting pixel activation lines from the substrate." JCC, Ex. B, pp. 10-11. Based on agreements and arguments by LGD and CPT in the prior case, this limitation is directed to the "***removal of*** the guard ring and row and column interconnections from the display panel (emphasis added)" and "***physical removal of*** the outer guard ring (emphasis added)." *See* Chen Decl., Ex. 3, Judge Farnan Memorandum Order, pp. 7, 9. For reasons set forth in AUO's Opening Brief and the JCC, AUO's proposed construction should be adopted should the Court decide to construe this limitation. *See* AUO Brief, pp. 39-40.

D. '449 Patent

The dispute between the parties focus on two limitations: (1) the "wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor" limitation[13] from claim 1; and (2) the "gate pad"/ "source pad" limitation from claims 10 and 11. LGD argues in its opening brief that the former limitation should be construed exactly the same as the construction provided by the California Court in the CPT California litigation, but that the latter limitation should receive a different construction than the California Court provided. LGD's inconsistent adoption of these prior constructions is wrong in both instances.

1. "[Wherein] one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor" (claim 1)

a. This limitation needs to be construed as a single phrase instead of small sub-limitations

As an initial matter, both AUO and CMO contend that this limitation should be construed as a single phrase. *See* AUO Brief, 41-42; CMO Brief, 20-23. LGD has chosen instead to construe the sub-limitation(s) "one of said first and second conductive layers" or "one" within the phrase. LGD Brief, 16-18. AUO's approach is congruent with the intrinsic record. In fact, the Applicant amended the claims by adding the wherein clause in its entirety to several independent claims during the prosecution of the '449 Patent. Joint Ex. C1 (file history for the '449 Patent), 12/01/97 Amendment at 1-4. LGD's approach might be appropriate had the Applicant added only short phrases such as "one of said first and second conductive layers," but this is not the case.

---

[13] LGD has chosen to construe sub-limitation(s) "one of said first and second conductive layers" or "one." For the reasons stated in II.D.1.a. AUO believes that this limitation should be construed in its entirety instead of small sub-limitations.

b. The prior construction in the CPT California litigation of the wherein limitation is not binding on the AUO Defendants

LGD relies on the prior Markman opinion from the California Court to support its contention that the term "one of said first and second conductive layers" should be construed as "one, but not both, of the first and second conductive layers." LGD Brief, 17-18. It is well established, however, that a prior construction by one court does not bind an independent defendant litigating in another court. *See, e.g., Texas Instruments, Inc. v. Linear Techs. Corp.*, 182 F.Supp.2d 580, 585-87 (E.D. Tex. 2002) (held that construction of the same claim limitations by a prior court is not binding on an independent defendant).

c. The prior construction in the CPT California litigation of the wherein limitation is based on an erroneous interpretation of the file history

The short explanations[14] provided by the California Court in its opinion construing this phrase indicate that the California Court's reasoning was based on an incorrect understanding of the file history. Specifically, the California Court's opinion noted the following:

> In the instant case, patentee specifically disavowed an interpretation of the claim that provided for either, or both – in other words, "one of more" – of the conductive layers being connected to a terminal of thin film transistor; in December 1997, in order to obviate an obviousness rejection, LGE patent applicant Woo Sup Shin specifically amended the claim to articulate the "one of said first and second layers" limitation. The Court, therefore, finds that the term "one" in Claim 1 means "a single layer."

LGD's Ex. L-6(e) at 2.

[14] The summary manner by which the construction was handled by the California Court and the parties is likely due to the late submission of the issue to the California Court. The Markman briefings were submitted to the California Court on the eve of the trial; and the opinion was issued as a minute order from the chambers during the course of the trial.

The Applicant's amendment, which adds the wherein limitation to several independent claims, was not an explicit disavowal, however. Indeed, the Applicant did not need such a disavowal to overcome the examiner's obviousness rejection based on prior art reference Kakuda. *See* LGD Brief, p. 17. The Applicant contended that Kakuda does not teach the wherein limitation because its conductive layer is connected to either a "storage capacitor" or some "external connection terminal." Joint Ex. C1 (file history for the '449 Patent), 12/01/97 Amendment at 5-6. In other words, neither the first nor the second conductive layer in Kakuda is connected to a terminal of a thin film transistor. *Id* at 6. The statements the Applicant made therefore do not support the California Court's conclusion that there was a specific disavowal.

d. The prior construction in the CPT California litigation contradicts clear teachings of the intrinsic record

In addition to misinterpreting portions of the '449 file history, the California Court's construction is further flawed because it overlooked critical aspects of the patent specification and the prosecution history. First, as Defendants' opening brief points out, the California Court's construction overlooked an important embodiment (Figs. 4 and 5) disclosed in the patent. AUO Brief, 41-42. *See also* CMO Brief, 22-23. Second, the construction failed to reconcile the remarks made by the Applicant during the prosecution, which indicated, at a minimum, that the wherein clause in claim 6 of the '449 Patent should be interpreted to mean "one or more conductive layers is connected to a plurality of TFT terminals." AUO Brief, 41-42; CMO Brief, pp. 20-22. The file history provides no reason to construe the wherein clause in claim 1 differently from that of claim 6. *See* CMO Brief, 21 (contending that the scope of the two phrases should be the same based on the file history). "Unless otherwise compelled, when different claims of a patent use the same language, we give that language the same effect in each claim." *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1118-19 (Fed. Cir. 2004).

e. The prior construction in the CPT California litigation is further inconsistent with the open-ended "comprising of" language

Finally, AUO's construction is fully supported by the open-ended language of the term "comprising." *Scanner Techs Corp. v. ICOS Vision Sys. Corp.*, 365 F.3d 1299, 1304 (Fed. Cir. 2004) ("This court has repeatedly emphasized that an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'") (internal citation omitted). *See also Lampi Corp. v. Am. Power Product*, 228 F.3d 1365, 1376 (Fed. Cir. 2000) ("The proper interpretation of the 'housing having two half-shells' limitation is a 'housing having at least two equal or corresponding parts forming a hard or firm outer covering into which the housing of the fluorescent lamp is divided.'").

f. "connected to" sub-limitation

A remaining issue is how to construe the sub-limitation "connected to." AUO submits that the term be construed as "electrically connected", while LGD contends that the term means "directly connected to." LGD's construction reads solely on one preferred embodiment (Fig. 3), and is therefore unnecessarily restrictive. AUO submits that the term "connected to" should be construed broadly to encompass both directly connected *and* connected via intervening elements. To avoid any confusion, AUO is willing to modify its proposed construction to read "either electrically connected or physically connected."[15]

2. "Gate pad"/"Source pad" (claims 10 and 11)

The main difference in the parties' constructions lies in whether the gate/source pads encompass the entirety of "patterned, electrically conductive material provided near the

[15] AUO's proposal differentiates the term "connected to" with "electrically connect" as the former is broader in scope than the latter.

periphery of the thin film transistor …", or only a portion of the "patterned, electrically conductive material."[16]

Not only is there no intrinsic support to limit gate/source pad to only "a portion of" of the "patterned, electrically conductive material provided near the periphery of the thin film transistor array to receive gate/source signals from a gate/data driving circuit," AUO Brief, 43, LGD's narrow construction is illogical. If only a portion of "patterned, electrically conductive material [that receives] gate signal from a gate driving circuit" constitutes a gate pad, there is no explanation for the remaining portions of the "patterned, electrically conductive material." Further, LGD does not describe, nor is there any basis for how one of ordinary skill in the art would decide, which portion of the patterned material is gate pad and which portion is not.

E. '274, '321, and '489 Patents

The claim construction issues with respect to the '274 Patent Family fall into two groups. First, what characteristics must the claimed structure possess. (The "claimed structure" in the '274 Patent is a "double-layered structure" and in the '321 and '489 Patents a "double-layered metal gate"). Second, how does one determine the width (if one can) of the first and second metal layers of the claimed structure. The proposed constructions of AUO and CMO are largely in agreement on these issues; LGD's constructions, however, either ignore these issues entirely or offer definitions that lead to absurd results. AUO respectfully requests that the Court adopt its proposed constructions.

---

[16] AUO's proposal is "a patterned, electrically conductive material provided near the periphery of the thin film transistor array to receive gate/data signals from a gate/data driving circuit." LGD's proposal is "a portion of the patterned, electrically material provided near the periphery of the thin film transistor array to receive gate/data signals." *See* JCC, Ex. C. LGD's proposal omits the recitation of "from a gate/data driving circuit," which was part of the prior construction from the California Court.

1. Characteristics of the Claimed Structures

While the claim terms at issue might, in a vacuum, seem to be broad, a review of the patent specification and file history makes clear that the patents are addressed to thin film transistor structures with two key features: 1) two layers, and 2) at their edges, the layers have a stepped structure with each other and with the substrate on which they rest.

LGD does not dispute that the "double-layered" structure of the claims must have two layers, but argues that the claim language allows for a structure having more than two layers. *See* LGD Brief at p. 23. This is belied by the patentee's choice of the term ***double***-layered, which denotes two layers, rather than the term ***multi***-layered, which might have allowed for more than two layers. Likewise, even if one considered the use of the term "including" in the claims to allow for additional features, that word is used to indicate that the gate (of which the double-layered structure is a part) may have additional features.[17] The fact that a particular structure may be only one of many parts of a gate does not mean that the structure can be something other than what the claim language clearly states: a double-layered structure.

Likewise, the patent makes clear that the invention relates not to any structure with two layers, but to structures with those two layers arranged in a step structure. The patent discloses only structures in which the two metal layers form a "double step difference" between the substrate and the top of the structure. *See* '274 Patent at Figs. 3, 4C, and 1C. Indeed, the purpose of the invention was to improve step coverage "in such a structure having a double step difference between the substrate and the gate." *Id.* at 4:40-52. The size of these "double step differences" were explicitly claimed and described as one of the novel features of the patent. *Id.*

---

[17] Interestingly, while LGD grasps at the open ended term "including" in the ''274 Patent Family, it asks the Court to ignore the equally open-ended term "comprising" in the '449 Patent. *Cf.* LGD Brief at pp. 16-18.

at 5:30-34. The explicit claim limitations directed to the widths of the first and second metal layers necessarily result in the creation of a double step structure. Thus, one reading the patent would understand the "double-layered structure" to be arranged in a step structure.

This is further borne out by the prior art that was cited during prosecution, and on which the invention claimed an improvement. The Wei and Miyago references cited by the patent examiner show double step structures. *See* Chen Decl., Exs. 6 and 7. The specification also recognized that double step structures were the prior art relevant to the invention. '274 Patent at 1:39-43; 2:5-8.

Finally, LGD's proposed construction of "a second metal layer disposed on the first metal layer" both goes too far and not far enough. By imposing that the two metal layers be "sequentially deposited," LGD introduces an unnecessary process requirement into what is clearly an apparatus claim. On the other hand, by simply repeating the word structure without defining what the structure must look like, LGD ignores the intent of the patent to address a specific type of structure. For each of those reasons, LGD's construction should be rejected.

The Court should construe these terms in the full context of the disclosure and prosecution history, and adopt AUO's proposed construction.

2. Width of the Metal Layers

a. The '274 Patent Family does not teach where to measure the width, and is therefore indefinite.

The '274 Patent Family requires the difference in width between the first and second metal layers fall within a specific numerical range. When a patent "includes a numeric limitation without disclosing which of multiple methods of measuring that number should be used" it is indefinite. *Halliburton Energy Serv., Inc. v. M-I LLC*, 514 F.3d 1244, 1249 (Fed. Cir. 2008); *Honeywell Int'l, Inc. v. ITC*, 341 F.3d 1332, 1340 (Fed. Cir. 2003). The '274 Patent Family does not disclose where each of the metal layers should be measured when determining its width.

This is particularly important since the patent contemplates the layers having sloped edges, which would mean that the width would be different when measured at the top surface or the bottom surface. *See* '274 Patent at 6:12-14; Figs. 3, 4C, and 4F.

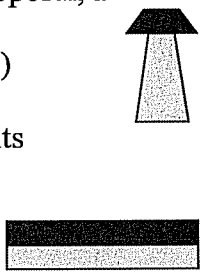
The indefiniteness of the claims is highlighted by the parties varying proposals for what would be the proper place to measure. AUO believes that both metal layers should be measured at the surface where they meet. CMO proposes that both layers should be measured at their top surface. LGD (in a departure from any ordinary understanding of the word "width") contends that the measurement should include both the top surface and the sides of the first metal layer. The fact that each of the possibilities (as well as others) exists from the disclosures of the '274 Patent Family demonstrates that the patents do not clearly dictate how the measurement is to be performed. Because the measurement of the metal layers is critical to determining whether the claim limitations are met, and because the different possible measurements would give different results, the claims fail to clearly identify the bounds of the invention and are indefinite. *See Honeywell*, 341 F.3d at 1341.

b. LGD's proposed constructions lead to nonsensical results.

Not only does LGD ignore the fact that the '274 Patent family does not teach where to measure the width of the layers, it proposes a construction of these terms at odds with any commonly accepted understanding of the term width. Instead, LGD proposes that the width of the first metal layer includes both the portion of the first metal layer in contact with the second metal layer ***and*** the portions of the first metal layer exposed to the gate insulating layer. In other

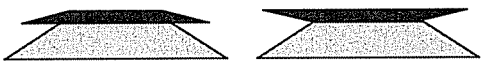
words, LGD maintains that the width of the first metal layer is determined by measuring the distance of both the top surface and the sides of the first metal layer.[18]

Such a construction quickly leads to nonsensical results. Under LGD's proposal, a structure such as shown here would be considered to have a first metal layer (gray) "wider" than the second metal layer (black), even though the first layer (gray), at its widest point, is smaller than the second layer (black) at its smallest point.



Likewise, in a structure where both layers are rectangular, in which any ordinary person would consider the layers to be of the same width, LGD's construction would say that the first metal layer is wider, because of the sides that would still be exposed to the gate insulating layer. Indeed, LGD's position would allow one to increase the "width" of the first metal layer simply by increasing its thickness. There is no basis in the '274 Patent Family to indicate that the patents take such a radically different view of the commonly understood word "width", and LGD's construction should therefore be rejected.

Further LGD's construction would allow embodiments that are directly in conflict with the '274 Patent Family's stated purpose of providing improved step coverage. *See* '274 Patent at 3:21-25. By including all of the exposed portions of the first metal layer within its definition of "width", LGD's proposal would allow the first metal layer to be considered wider than the second metal layer, but to be configured in a manner that would dramatically diminish step coverage by the later insulating layer. For example, structures such as shown here could have a first metal layer (gray) and a second metal layer (black) that purportedly satisfied the claims, but



[18] LGD's attempt to rewrite the term "width" is related to its improper attempt to conflate the term "side/side portion" with "thickness". As demonstrated in AUO Brief, the patentee understood and used the terms distinctly. *See* AUO Brief at pp. 45-46.

would provide worse step coverage when an insulating layer was deposited from above. These further nonsensical results demonstrate the incorrectness of LGD's position.

3. Claim 10 of '321 Patent is indefinite

It is undisputed that the term "first etching layer" in Claim 10 does not have any antecedent basis. To avoid the resulting indefiniteness, LGD must ask this court to judicially correct the claim and rewrite the term to be "first ***metal*** layer." The Court may do this only if there is only one possible correction for the claim term, and it is obvious from the face of the patent. *See Group One Ltd. v. Hallmark Cards, Inc.*, 407 F. 3d 1297 (Fed. Cir. 2005). Here, it is unclear whether the term etching layer was intended to be metal layer, or whether an etching layer (which would have provided the antecedent basis) was omitted from Claim 7. Without judicial correction, the term lacks antecedent basis and the claim is therefore indefinite. *See Energizer Holdings, Inc. v. Int'l Trade Comm'n*, 435 F.3d 1366, 1370-71 (Fed. Cir. 2006).

F. '569 Patent

Again, several disputed terms were not addressed by LGD or CMO in their opening claim construction briefs.[19] As set forth in AUO's opening claim construction brief and JCC chart, AUO's proposed constructions for these terms are the proper ones and should be adopted.

1. "the gate line having an opening therein" (claim 17) and "the gate electrode having an opening therein" (claim 25)

LGD's shifting arguments are apparent here. On one hand, LGD asks this Court to import, and in fact replace, the structural limitations of the apparatus claims 17 and 25 with functional limitations described in specific embodiments of the '569 Patent. *See* LGD Brief, p.

[19] The claim terms the other parties failed to address for the '569 Patent include "a gate line" (claims 17 and 25)", "a first electrode" (claim 25), "a second electrode" (claim 25) and "a third electrode" (claim 32),"a semiconductor layer on the first insulating layer over at least a portion of the opening" (claim 7), and "a drain electrode on the semiconductor layer over at least a portion of the opening" (claim 17).

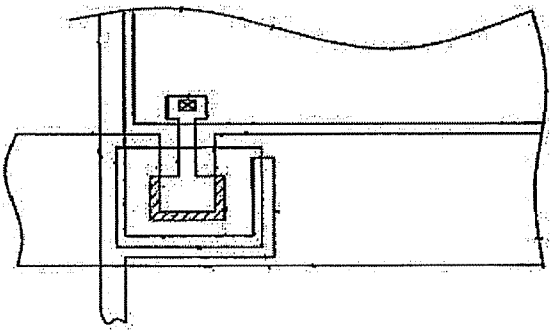
27 (first paragraph). On the other hand, LGD accuses AUO of importing limitations from the '569 Patent by mischaracterizing AUO's proposed construction. *Id.* (second and third paragraphs).

The plain meaning of the claim terms at issue is clear, and the meaning denotes structural characteristics. The claims in the '569 patents are apparatus claims and are comprised of structural limitations. In fact, nowhere in any of the thirty-seven claims does even one word suggest any of the functional limitations LGD now wishes to import. LGD essentially asks this Court to rewrite the claims, which should not be permitted. *See Ecolab, Inc. v. Environchem, Inc.*, 264 F.3d 1358, 1367 (Fed. Cir. 2001); *Transmatic v. Gulton Indus.*, 53 F.3d 1270, 1278 (Fed. Cir. 1995) (rejecting an attempt to limit a claim "by importing unnecessary functional limitations into the claim," i.e., lighting fixtures are deemed not limited to those that attach to public transit vehicles ***in a certain way*** because the claim language itself contained no such functional limitation).

Contrary to LGD's assertions, AUO's proposed construction is not limited to the narrow structures described in the various figures of the specifications. In fact, AUO's proposed construction is proper because it follows the consistent teachings of the '569 Patent regarding the structural characteristics—such as the shape and structure of the opening, the electrode, and most importantly, the overlap—and merely seeks to clarify the ***structure*** of the structural claim limitation based on those consistent teachings. Specifically, AUO's proposes as the construction of opening "a cut out extending from the periphery of the gate line to the interior of the gate line." AUO's proposed construction does not require that the opening retain a rectangular or inverted T shape, as are shown in the figures of the patent. Many shapes could satisfy this construction: a non-inverted T, dome, square, trapezoid, or round shaped opening, to name just a few. Rather than adding specific shape requirement (as LGD accuses), AUO's proposed

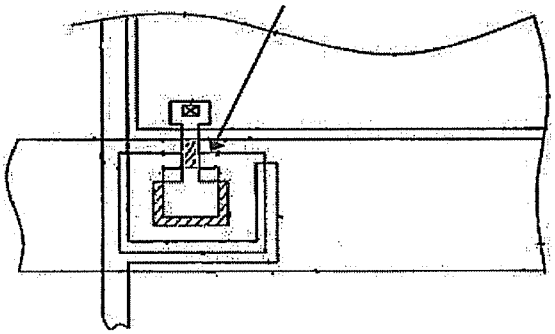
construction recognizes the consistent teaching of the ***structural*** characteristics within the '569 Patent that the opening is a cut out that is "vertically elongated from a top edge to a center of the gate line," *see* '569 Patent at 6:31-41, so that the inventive aspect of having gate electrode overlap by only the edges of the drain electrode can be achieved. *See, e.g.*, '569 Patent, Abstract, 4:63-65, 6:13-15, 8:7-10, 7:13-18, 8:34-35; Fig. 8 ("overlapped area (depicted by oblique lines) is formed on both end sides of the drain electrode 117."). If a hole is formed in the gate line instead of an opening, then the gate electrode would overlap more than just the edges of the drain electrode (as shown below in the figure on the right), creating effects described as undesirable and not intended by the teaching of the '569 invention:

("Opening" of the '569 patent create inventive overlap at only the edges of drain electrode)



V.

(A hole would create undesirable overlap at second electrode portion (in yellow))

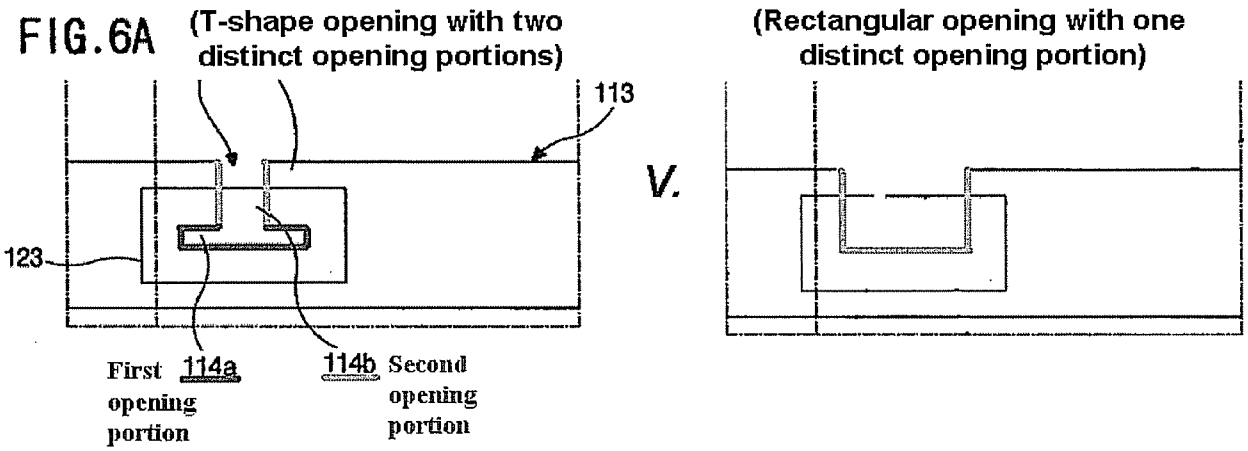


This is consistent with the '569 Patent's teaching that the second electrode portion (highlighted in yellow above) does not overlap the gate electrode. *See* '569 Patent at 7:13-18.

Because LGD's proposed construction seeks to improperly incorporate functional limitations into an otherwise structural limitation, the Court should adopt AUO's proposed construction that captures the plain meaning and is amply supported by the specification.

2. "the opening includes a first opening portion and a second opening portion," "a first opening portion," and "a second opening portion" (claim 25)

Once again, the Court should reject LGD's attempt to add functional limitations to these "opening portion" limitations. There is no dispute that the specification describes both a rectangular-shaped and an inverted T-shaped opening. However, it is clear that that the specification associates the two distinct opening portions only with the "inverted T-shaped" opening, and not the rectangular-shaped opening. *See* '569 Patent at 8:40-45, 4:48-53, 6:32-41, 7:6-19.



A rectangular-shaped opening (shown above on the right) would not have two separate and distinct opening portions. *See id.* at 8:40-45. Plainly, the specification and the claims make a distinction between a shape, such as a rectangle, square or a circle, that does not have two separate and distinct opening portions with a shape that does, such as a T-shaped, non-inverted T-shaped, or L-shaped opening. AUO's proposed construction follows the plain meaning and captures, structure-wise, the consistent teaching of the '569 Patent, including the non-rectangular shape with the two distinct opening portions

3. "substantially surrounds the drain electrode" and "substantially" (claim 21)

While LGD argues in another context that the every day English word "substantially" could mean both "all" and "nearly all," *see* LGD Brief, pp. 8-9, LGD now contends that the same word should only mean "considerably" here. In contrast, not only is AUO's proposed construction of "surrounds almost all the drain electrode portion" the same as the construction of "almost all" AUO proposed, but it also better captures the plain meaning of "substantially" enclosing on all sides and is consistent with the teaching of the '569 Patent. *See* AUO Brief, p. 53. Attempting to manufacture support for "considerably," LGD argues that because only the lower portion of the drain electrode is surrounded by the source electrode, the ***entire*** drain electrode cannot be almost all surrounded. (Implicit in LGD's arguments is LGD's admission that the "drain electrode ***portion***" indeed is almost all surrounded by the source electrode.) However, the parties are not disputing whether the ***entire*** drain electrode is surrounded, but whether a drain electrode "portion" is. Since there is no real dispute, the court should adopt AUO's more consistent and clear proposed construction.

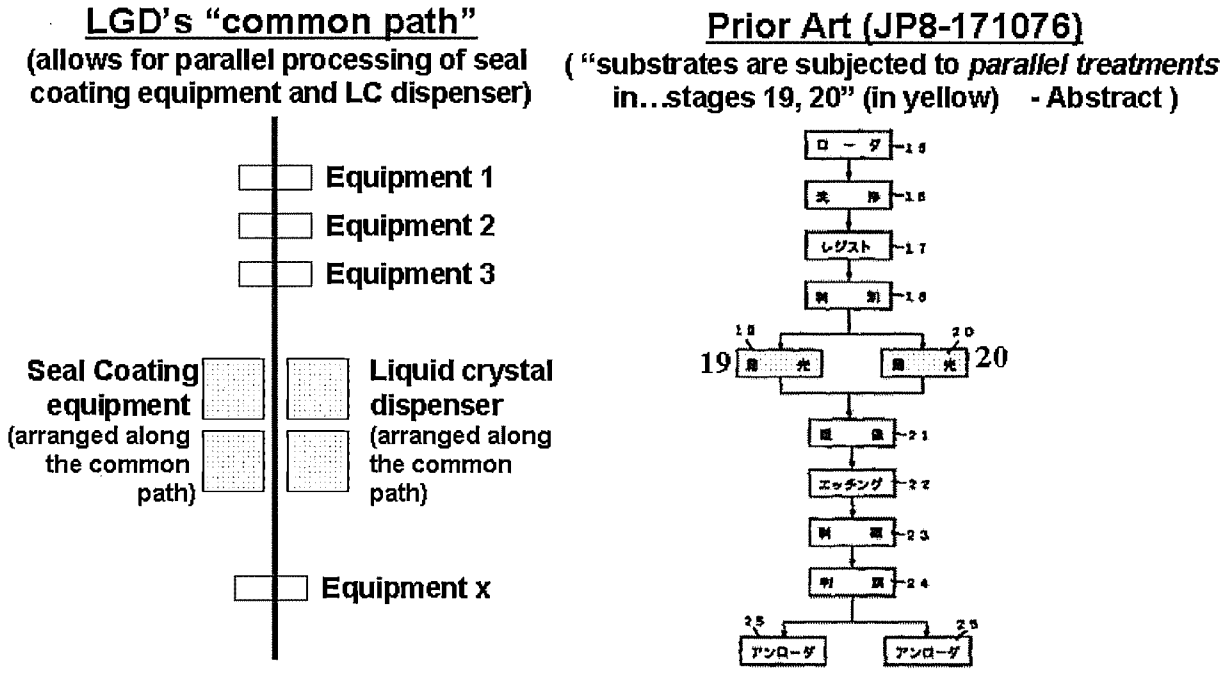
G. 984 Patent

1. "on a single production process line" (claim 1)

There is no dispute that both LGD's and AUO's proposed constructions for the terms in claim 1 recognize that the claimed "single production process line" is formed by various "processing equipment/machines" on that line. LGD directly incorporates "processing equipment/machine" in its construction for "on a single production process line," while the Defendants incorporate "processing equipment/machine" in their constructions for the "sealing material coating/liquid crystal dispensing portion of [this] single production process line." JCC, Ex. E, pp. 2-3, 5. This mutual recognition is entirely consistent with the specification teaching of the "processing equipment" of the production line to include "equipment for the TFT substrate,

equipment for the color filter substrate or both," "a seal dispenser," and a "LC [(liquid crystal]] dispenser." *See* '984 Patent at 5:26-32, 2:54-56, 2:63-66.

However, instead of proposing a construction that reflects the spatial arrangement of the "processing equipment/machines" and its processing flow, as dictated by the claim term and the teaching of the specification, LGD ignores this aspect of the invention entirely. LGD's proposal of "processing equipment [] arranged along a common path" is so general that it encompasses various different types of arrangements and flows, including "parallel processing" along this "common path" as well as branch processing from such "common path." This directly contradicts the clear teaching of the single line structure and processing of the '984 Patent, as well as the remaining claim language. Indeed, the "Summary of the Invention" section requires that the pair of opposite substrates pass through the same seal dispenser and the same LC dispenser. *See* AUO Brief, p. 55; *see also* '984 Patent at 3:61-4:13. LGD's construction would also impermissibly encompass the parallel arrangement processing that the patentee disclaimed in overcoming the prior art. *See* AUO Brief, p. 55.



Importantly, the '984 Patent specifically teaches against any type of parallel and branch processing within the single production process line, so that "problems caused by" having two parallel processes is avoided, "spatial efficiency" is achieved, and "productivity" is increased. *See* '984 Patent at 7:35-42, 5:23-25. As the patentee points out in the "Background" section, "parallel" processing will result in extra equipment, loss of spatial efficiency, and a decrease in productivity due to differences in processing times for the two opposite substrates. *See* '984 Patent at 3:25-43. Because AUO's proposed construction flows directly from the plain meaning and matches the spatial arrangement, processing flow, and purpose of the alleged invention, AUO respectfully requests that the Court adopt its construction. JCC, Ex. E, p. 2.

2. "passing the first and second substrates through a sealing material coating portion of the single production process line in serial order" and "a sealing material coating portion of the single production process line" and "in serial order" (claim 1)

While mischaracterizing the "principle differences" between the parties' construction, LGD conveniently leaves out the highly contested language "passing…through" from this disputed term. However, there is no basis for LGD to broaden the claim scope by disregarding the limitation "passing…through." Doing so actually contradicts the plain meaning of passing something in one side and out the other. *See* CMO Brief, Ex. E-5. The specification teaches that the pair of opposing substrates pass "through" the same sealing dispenser, followed by passing the pair through the same LC dispenser and out to the assembling chamber. *See* '984 Patent at 4:14-25, 6:19-41. As the substrates are passed through, the serial order of the pair of opposing substrates is maintained throughout the process. *See* '984 Patent at Fig. 2-4; *see also* AUO Brief, pp. 56-57.

LGD's quibble with "sealing material coating portion of the single production process line" is puzzling at best, as LGD shifts between "equipment" and "portion" within the same claim. As discussed in Section G.2 above, all parties have already recognized that the "single

production process line" is formed by various "processing equipment/machines" on that line, including a "seal dispenser," a "LC dispenser," "equipment for the TFT substrate," "equipment for the color filter substrate," and equipment for "both." *See* '984 Patent at 5:26-32, 2:54-56, 2:63-66. The seal dispenser is the machine that dispenses the seal in the production process line, *id.* at 2:54-56, and according to the claim invention, both opposing substrates must pass through the "sealing material coating step" carried out by the seal dispenser. *Id.* at 6:32-35. The same holds true for the "[LC] dropping step," as the pair of opposing substrates must also pass through that step carried out by the LC dispenser, *id.* at 6:39-41, which is the machine that dispenses the liquid crystal in the production process line. *Id.* at 2:63-66. While LGD's intention in the sudden shift from "equipment" to "portion" is unclear, LGD's proposed construction seemingly allows the scenario in which the pair of opposing substrates can pass through a "sealing material coating ***portion***" without passing through the actual seal material coating equipment—i.e., the "seal dispenser." This is in direct conflict with the patent, and further contradicts the position that the patentee took to differentiate its invention from the prior art during prosecution.[20]

Similarly, LGD's criticism of AUO's proposed construction on "in serial order" is ill founded. Construing the term as "one after the other without anything in between," as AUO proposed, is entirely proper in view of the plain meaning of the word "serial." *See*, *e.g.*, Second Chen Decl., Ex. 4, THE AMERICAN HERITAGE DICTIONARY 747 (3rd Ed. 1994) ("serial" defined as "Of, forming, or arranged in a series"; "series" as "A number of objects or events arranged

---

[20] Faced with the "Admitted Prior Art" and JP8-171076, the patentee made clear that its invention is different because the pair of opposing substrates pass through the claimed "sealing material coating portion" without the sealing material coating process being performed, while in the prior art, "if a substrate passes through a process portion, the corresponding process is always performed." Joint Ex. E1 (file history for the '984 Patent), 1/6/04 Response at p. 4. There is no question that the claimed "process portion" is the equipment that performs the corresponding

(continued...)

one after the other in succession; set."); *accord Labratories Perouse v. W.L. Gore & Assocs.*, 528 F.Supp.2d 362, 390-91 (S.D.N.Y. 2007) (endorsing Plaintiff's view that the term "a series of gussets" be construed as gussets "come one after another in spatial succession."). AUO's proposal is also supported by the patent itself, which makes clear that the pair of opposing substrates is provided without anything in between. These two substrates, described as a "pair," are "alternately provided into a production line" and "pass through each component of production process line." *See* '984 Patent at 7:25-33; 5:23-30. Using "alternately" demonstrates that first one, then the other, substrate is put into the production line; simply put, there could be nothing between a "pair" of alternating substrates.

Together, AUO's proposed construction of "providing the first and second substrates one after the other, without anything in between; in at one end, and out at the other end in the same order of a equipment/machine for coating sealing material on a substrate in the single production process line" correctly captures the terms' plain meaning and is consistent with the patent's description of "passing…through," "sealing material coating portion of the single production process line," and "in serial order."[21] JCC, Ex. E, pp. 3-5.

(...continued from previous page)

step, which in this case is the coating of the sealing material by the "seal dispenser" in the production process line. *See* '984 Patent at 2:54-56.

[21] The same analysis also applies to construction of the claim limitation directed to the LC dispenser of the production process line: "passing the first and second substrates through a liquid crystal dispensing portion of the single production process line in serial order" (claim 1). Consequently, for the same reasons set forth above, the Court should construe this limitation for LC dispenser similarly. *See* JCC, Ex. E, p. 5. Notably, LC dispenser "receive[s] the first and second substrates in serial order" and processes one of them, and then the assembler "receive[s] the first and second substrate" in the same order. *See* '984 Patent at 4:20-30.

H. '374 Patent

LGD's opening brief disputes AUO's proposed construction for three limitations: (1) "forming a main sealant;" (2) "wherein the auxiliary sealant and the main sealant are contiguous;" and (3) "preparing a lower and an upper substrate." With the exception of the third limitation, which AUO contends is indefinite, LGD's proposed constructions invariably and impermissibly import limitations from the preferred embodiment which is contrary to the plain meaning of the claim language. *Liebel-Flarsheim v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) ("[T]his court has expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.")

1. "Forming a main sealant" (claim 1)

a. LGD's proposal impermissibly limits the term "forming" to "depositing"

Because the verb "form" has a meaning that is readily apparent to a lay person,[22] *Phillips*, 415 F.3d at 1314 (claim construction could involve little more than the application of the widely accepted meaning of commonly understood words. in cases where "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges"), AUO submits there is no need to construe the term.

LGD contends, however, that "form" should be construed as "deposit," because the specification teaches only depositing sealant. LGD Brief, 30. LGD's proposal therefore reads out forming a sealant via screen printing. *Id.* LGD is flatly wrong. As a matter of fact, the specification specifically notes that a sealant can be "formed" by both a dispensing method (depositing) and screen printing method. '374 Patent at 2:21-22.

---

[22] "Form" means "to give a particular form or shape to." Second Chen Decl., Ex. 2, RANDOM HOUSE WEBSTER'S COLLEGE DICTIONARY 523 (1991).

b. LGD's proposal improperly requires that the main sealant has to "fully" enclose the liquid crystal display region[23]

LGD's opening brief also impermissibly imports the features of the preferred embodiment into the construction of the term "main sealant." While the preferred embodiment in Fig. 3B of the '374 Patent shows a main sealant fully enclosing the liquid crystal within, a segment of sealant that does not fully enclose but performs the function of confining the liquid crystal within constitutes a main sealant nevertheless. This understanding is reflected by the examiner's remarks made during the prosecution of the '374 Patent. The examiner, for example, specifically references a sealant pattern that does not fully enclose in a piece of prior art (Furushima) as main sealant. Joint Ex. I1 (file history for the '374 Patent), 12/01/03 Office Action at 3. (Element 3 in Fig. 4 of Furushima). *See also* Second Chen Decl., Ex. 3, U.S. Patent No. 5,410,423) (Furushima), Fig. 4(3).

2. "Preparing a lower and an upper substrate" (claim 1)

Contrary to LGD's assertions, AUO contends that this limitation is indefinite because it does not specify with particularity what steps or processes are involved in preparing a lower and an upper substrate. In addition, it does not delineate where a "preparing" step begins and where a "preparing" step ends. LGD contends that the meaning of the phrase has a straightforward meaning to one of ordinary skill in the art. LGD Brief, 32. LGD provides no evidentiary support for this statement, however. LGD offers no expert declaration, no inventor testimony, no dictionary definitions, and no cites to learned treatises. Furthermore, LGD's proposal, which recites "making the substrates ready for depositing sealant and liquid crystal material prior to attachment," does not specify what steps or processes are performed on the substrates to make

[23] AUO further contended on its opening brief the main sealant's function is to enclose liquid crystal instead of the display area. AUO Brief, p. 59.

them ready for the processing steps recited in the following limitations in the claim. In short, one reading the '374 Patent would have no way of knowing what constituted preparing and thus no way of know the scope of the claimed invention. This term is therefore indefinite. *See Halliburton*, 514 F.3d at 1249.

Dated: September 4, 2008

/s/ Karen L. Pascale

Richard H. Morse (#531)
John W. Shaw (#3362)
Karen L. Pascale (#2903)
Andrew A. Lundgren (#4429)
YOUNG CONAWAY STARGATT & TAYLOR LLP
The Brandywine Building
1000 West Street, 17th Floor
P.O. Box 391
Wilmington, DE 19899-0391
(301) 571-6600
kpascale@ycst.com

Attorneys for AU Optronics Corporation and AU Optronics Corporation America

OF COUNSEL:

Vincent K. Yip
Peter J. Wied
Terry Garnett
PAUL HASTINGS JANOFSKY & WALKER LLP
515 South Flower Street, 25th Floor
Los Angeles, CA 90071
(213) 683-6000

M. Craig Tyler
Brian D. Range
WILSON SONSINI GOODRICH & ROSATI
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, TX 78759-8497
(512) 338-5400

Ron E. Shulman
Julie M. Holloway
WILSON SONSINI GOODRICH & ROSATI
650 Page Mill Road
Palo Alto, CA 94304-1050
(650) 493-9300

CERTIFICATE OF SERVICE

I, Karen L. Pascale, Esquire, hereby certify that on September 4, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

Richard D. Kirk [rkirk@bayardfirm.com]
Ashley B. Stitzer [astitzer@bayardfirm.com]
BAYARD, P.A.
222 Delaware Avenue, Suite 900
P.O. Box. 25130
Wilmington, DE 19899-5130
(302) 655-5000
Attorneys for LG Display Co., Ltd. and LG Display America, Inc.

Philip A. Rovner [provner@potteranderson.com]
David E. Moore [dmoore@potteranderson.com]
POTTER, ANDERSON & CORROON
6th Floor, Hercules Plaza
1313 N. Market Street
Wilmington, DE 19801
Attorneys for Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc.

I further certify that I caused a copy of the foregoing document to be served by e-mail on the above-listed counsel of record and on the following non-registered participants in the manner indicated:

By E-mail

Gaspare J. Bono [gbono@mckennalong.com]
Matthew T. Bailey [mbailey@mckennalong.com]
R. Tyler Goodwyn, IV [tgoodwyn@mckennalong.com]
Lora A. Brzezynski [lbrzezynski@mckennalong.com]
Cass W. Christenson [cchristenson@mckennalong.com]
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, NW
Washington, DC 20006
(202) 496-7500
Attorneys for LG Display Co., Ltd. and LG Display America, Inc.

Jonathan S. Kagan [jkagan@irell.com]
Alexander C.D. Giza [agiza@irell.com]
IRELL & MANELLA LLP
1800 Avenue of the Stars
Suite 900
Los Angeles, CA 90067
(310) 277-1010
Attorneys for Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc.

YOUNG CONAWAY STARGATT & TAYLOR LLP

/s/ Karen L. Pascale

September 4, 2008

Richard H. Morse (#531) *[rmorse@ycst.com]*
John W. Shaw (#3362) *[jshaw@ycst.com]*
Karen L. Pascale (#2903) *[kpascale@ycst.com]*
Andrew A. Lundgren (#4429) *[alundgren@ycst.com]*
The Brandywine Building
1000 West St., 17th Floor
P.O. Box 391
Wilmington, Delaware 19899-0391
Phone: 302-571-6600
Attorneys for AU Optronics Corporation and AU Optronics Corporation America

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1: A process for producing a thin-film transistor comprising	a process for producing a thin-film transistor (C)		a method for manufacturing thin-film transistors such as for a liquid crystal display	plain meaning in light of the construction below for "thin-film" transistor	plain meaning
	thin-film transistor (C)	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	Plain meaning. Alternate: A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
a first step for forming a gate electrode on an insulating substrate,	forming a gate electrode on an insulating substrate (C)		giving form or shape to a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode that is above and supported by or in contact with material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation	plain meaning	Producing a gate electrode above, supported by, and in contact with an insulating substrate
	forming ... on (C)	Giving form or shape to … above and supported by or in contact with.	giving form or shape to...above and supported by or in contact with	plain meaning	Producing . . . above, supported by, and in contact with
	insulating substrate (C)	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation. [Previously Agreed upon Construction]	the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			insulation.	insulation	insulation
a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere,	continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film (C)	"on said gate electrode and substrate" means "above and supported by or in contact with the gate electrode and the insulating substrate." [Previously Agreed upon Construction]	the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film (without intervening films) above and supported by or in contact with (i) the patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode and (ii) the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.	construe the term: "depositing on said gate electrode and substrate" as: depositing above and in contact with the gate electrode and the insulating substrate	Precipitating a gate insulating film, a high resistivity semiconductor film and a conductive film on the gate electrode and the substrate without intervening films in between.
	continuously depositing (L, C, A)	The formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films.	the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films	The formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films.	Precipitating… without intervening films

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
	depositing on (C)		the formation of the gate insulating film the high-resistivity semiconductor film and conducting film above and supported by or in contact with	this term should be construed as part of the larger term "depositing on said gate electrode and substrate"	Precipitating above, supported by and in contact with
	depositing (A)		the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film	Plain meaning	precipitating
	gate insulating film (C)		a thickness of non-conductive material (such as SiNx) that has a high electrical resistance and insulates the transistor gate from the semiconductor.	a thickness of material (such as SiNx, SiOx, or a multi-layer film made of such materials) with a high electrical resistance, spanning the region from the gate electrode to the high resistivity semiconductor layer, for insulating the gate electrode from the channel	plain meaning or insulating film formed over the gate region
	high-resistivity semiconductor film (C)	A thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline	a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen- fluorine	A thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine	Plain meaning or Semiconductor having the property of high resistivity

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
		amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film	alloy, or a microcrystalline amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film.	alloy, or a microcrystalline amorphous silicon) that has a high resistance to current flow and acts as the channel region of the transistor	
	conducting film (C)	A thickness of electrically conductive material.	a thickness of electrically conductive material	A thickness of electrically conductive material that lies adjacent to the channel layer	plain meaning
	a conducting film containing at least a low-resistivity semiconductor film (L, C, A)	The conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films.	the conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films	Plain meaning The terms "conducting film" and "low-resistivity semiconductor film' should be construed separately from this term.	plain meaning
	low-resistivity semiconductor film (C)	A thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon, which contains phosphorous or other impurities to enhance the conductivity	a thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon which contains	A thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a low	Plain meaning or semiconductor having the property of low resistivity

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
		of the film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film.	phosphorous or other impurities to enhance the conductivity of the film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film.	resistance to current flow	
	without exposing them to an oxidizing atmosphere (C)		without exposing the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film to an atmosphere that would create a detectable amount of oxidation on a film.	Without permitting the gate insulating film, high-resistivity semiconductor film, low-resistivity semiconductor film, or conducting film to come into contact with an uncontrolled ambient atmosphere which contains oxidizing agents	Without exposing them to an atmosphere containing an oxidizing agent
	them (C)	The gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film. [Previously Agreed upon Construction]	the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film.	The gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film	indefinite
	oxidizing atmosphere (C)	An atmosphere that would create a detectable amount of oxidization on a film.	an atmosphere that would create a detectable amount of oxidation on a film.	an uncontrolled ambient atmosphere which contains oxidizing agents	atmosphere containing oxidizing agent
a third step in which	selectively etched (C)	The removal of selected	The removal of	Plain meaning	Selectively removed

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode,		portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.	selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.		or corroded by a chemical agent
	they are partly left as an island region on said gate electrode (L)		a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor	Plain meaning	indefinite
	island region on said gate electrode (C)	Portion of the conducting film, low-resistivity semiconductor film and high-resistivity semiconductor film which has been etched around its entire perimeter into a separate isolated region located over the gate electrode of a single thin-film transistor.	a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor.	Plain meaning	Isolated region above, supported by, and in contact with the gate electrode
	gate electrode (C, A)	A patterned, electrically conductive material that controls current flow through the channel	a patterned electrically conductive material that controls current	A patterned electrically conductive material that controls current	A patterned, electrically conductive material formed in the gate

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
		between the source electrode and the drain electrode.	flow through the channel between the source electrode and drain electrode	flow through the channel between the source electrode and drain electrode.	region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other	a fourth step for selectively forming a source electrode and a drain electrode (C, A)	Forming a source electrode and drain electrode in selected regions only.	forming a source electrode and drain electrode in selected regions only	Plain meaning	Step-plus function element. Function is "selectively forming a source electrode and drain electrode
	selectively forming (C)	Forming in selected regions only.	forming in selected regions only	Plain meaning	selectively producing
	source electrode (C, A)	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	construe term: "a source electrode and a drain electrode" as: Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and the drain electrode of the transistor under	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
				control of the gate electrode of the transistor.	
	drain electrode (C, A)	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode.	this term should be construed as part of the larger term "a source electrode and a drain electrode"	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
	contacting a part of the surface of said island region (L, C, A)	Touching a part of the surface of the island region.	touching a part of the surface of the island region	Touching a part of the surface of the island region.	plain meaning
a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask,	a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask (A)		a fifth step for removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask wherein the source electrode and drain electrode serve as at least a part of the pattern above a surface from which material is to be selectively removed; the pattern is made of material that is	eliminating all the conducting film in the space between the edges of the source and drain electrodes	a fifth step for using the source and drain electrodes to partially define the boundary for the removal of the conducting film exposed on the island region

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			resistive to the removal technique relative to the material to be removed		
	selectively removing said conducting film exposed on said island region (C)		removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask	eliminating all the conducting film in the space between the edges of the source and drain electrodes	plain meaning
	selectively removing (C)	Removing selected regions only.	removing selected regions only	This term should be construed as part of the larger term, "selectively removing said conducting film exposed on said island region."	plain meaning
	said conducting film exposed on said island region (A)		the conducting film on the island region that is not covered by the source electrode, drain electrode or mask	Plain meaning	the conducting film on top of the island region is exposed to the atmosphere
	said source and drain electrodes serving as at least a part of the mask (C, A)		the source and drain electrodes serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique	The source and drain electrodes are part of the pattern on the top surface that protects underlying layers from being removed while allowing the portion of the layer exposed between the source and drain electrodes to be	Using the source and drain electrodes to partially define the boundary for the removal or formation of the conductive film

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			relative to the material to be removed	removed	
	serving as at least a part of the mask (L)		serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask" see also construction of "mask" below	using … to partially define the boundary for the removal process
	at least a part of the mask (C)		at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed.	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask"	to partially define the boundary for the removal or formation process
	a part of the mask (A)		a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask"	to partially define the boundary for the removal or formation process

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			removal technique relative to the material to be removed.		
	mask (A)	A pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed.	A pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed.	A top surface pattern above one or more layers of material that will be selectively removed according to the shape of the mask. The mask is made of material that is resistive to the removal technique and defines by its edges the boundaries of the material selected for removal.	A pattern to define the boundary for the removal or formation process.
a sixth step for depositing a surface passivation film, and	surface passivation film (C)	A thickness of material that provides protection such as electrical stability and chemical isolation. [Previously Agreed upon Construction]	a thickness of material that provides protection such as electrical stability and chemical isolation.	Plain meaning	plain meaning
a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.	exposing a part of each of said source electrode, drain electrode and gate electrode (C, A)		removing portions of one or more layers to uncover a part of each of said source electrode, drain electrode and gate electrode	Plain meaning	causing a part of the source electrode, drain electrode and gate electrode to be exposed to the atmosphere
	exposing (A)		removing portions of one or more layers to uncover		Uncovering

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1: A method of manufacturing active matrix display backplanes and displays therefrom, comprising:					
providing a substrate;	Substrate (C)		the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	Plain meaning	plain meaning
forming a pattern of pixels on said substrate;	forming a pattern of pixels on said substrate (C)		depositing and etching a matrix of transparent electrically conductive material to form pixel electrodes above and supported by or in contact with the substrate	Forming a repeating configuration of redundant subpixels.	Forming a pattern of pixels above, supported by and in contact with the substrate
forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;	forming a plurality of row and column intersecting pixel activation lines (C)		depositing and etching electrically conductive material patterned in rows and columns that control pixels	Forming a plurality of row intersecting pixel activation lines and column intersecting pixel activation lines	forming a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines
	interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another (A)		electrically connecting with conductive material all or nearly all row lines to at least one other row line and electrically connecting with conductive material all or nearly all	Electrically connecting with conductors nearly all, but not all, of said row lines to one another and nearly all, but not all, of said column	joining almost all of the row lines together and joining almost all of the column lines together

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			of the column lines to at least one other column line	lines to one another.	
	Interconnecting (L, C)	Electrically connecting with conductors	electrically connecting with conductive material	Electrically connecting with conductors.	joining together
	substantially all (C, A)		all or nearly all	Nearly all, but not all.	almost all
	row lines (C)		electrically conductive material patterned in rows that control pixels	Indefinite or lines connecting all pixels in a row	indefinite; or lines connecting all pixels in a row
	Column lines (C)		electrically conductive material patterned in columns that control pixels	indefinite or lines connecting all pixels in a column	indefinite; or, lines connecting all pixels in a column
	row and column lines (C)		electrically conductive material patterned in rows and columns that control pixels	Indefinite or the row lines and the column lines	indefinite; or the row lines and the column lines

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and	outer electrostatic discharge guard ring (L, C, A)	A closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges.	a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharge	A closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges.	A surrounding structure outside the active matrix display to provide protection from electrostatic discharges
	resistance (L, C, A)	A circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from electrostatic discharge.	a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge	A circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge.	A circuit component that has a specified ratio between voltage and the flow of electric current, and used to minimize the current surge from electrostatic discharge.
	to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays (A)		to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display	Indefinite	To guard against electrostatic discharges between the row activation lines and column activation lines during the manufacturing of the displays
	protection from electrostatic discharges (C)		to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display	Indefinite	Plain meaning; or Guarding against electrostatic discharges
	row and column		electrically conductive	indefinite	Indefinite;

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
	activation lines (C)		material patterned in rows and columns that control pixels	or control lines activating all pixels in rows and control lines activating all pixels in columns	or Control lines activating all pixels in rows and control lines activating all pixels in columns.
removing said outer guard ring and row and column interconnections prior to completion of the display.	removing said outer guard ring and row and column interconnections (L, C)	Physically disconnecting said guard ring and row and column interconnections	physically disconnecting said guard ring and row and column interconnections	Physically disconnecting said guard ring and row and column interconnections.	Indefinite; Or physically disconnecting said guard ring and lines connecting the row and column intersecting pixel activation lines from the substrate
	Removing (A)		physically disconnecting said guard ring and row and column interconnections	Physically disconnecting	Taking away Alternate 1: separating or breaking off Alternate 2: physically disconnecting
Claim 8: The method as defined in claim 1 including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column	inner electrostatic discharge guard ring (L, C)		a closed or open ring, or open L or C-shaped line, inside the source and/or gate pads to provide protection from electrostatic discharge	A closed or open ring, or open L or C-shaped conductive line, inside the active matrix display to provide protection	Ring structure inside the active matrix display to provide protection from electrostatic discharges

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.				from electrostatic discharges.	
	shunt switching elements (C, A)		shunt transistors, including floating gate, no gate, an oxide below to form a spark gap, or other active switching elements such as diodes	An active switching element like a shunt transistor or diode.	A switching circuit for shunting electrostatic discharges

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1. A wiring structure comprising:	wiring structure (C)	A structure providing an electrically conductive path that connects at least two terminals.	a structure electrically connecting at least two points	A structure providing an electrically conductive path that connects at least two terminals.	a structure made by wires
a substrate;	Substrate (C)	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support. [Previously Agreed upon Construction]	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
a first conductive layer formed on a first portion of said substrate;	conductive layer (L, C)	A thickness of electrically conductive material. [Previously Agreed upon Construction]	thickness of electrically conductive material	A thickness of electrically conductive material that may include one or more patterned features, all of a single material.	plain meaning
	layer (C)		a thickness of material	plain meaning	plain meaning
	formed on a first portion of said substrate (C)		above and in contact with a first part of the substrate	above and in contact with a first part of the substrate	Produced above, supported by, and in contact with a first portion of the substrate
	formed on (C, A)	The Court construed "on" as "above and supported by or in contact with."	above and in contact with	above and in contact with	Produced above, supported by, and in contact with

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
a first insulative layer formed on a second portion of said substrate and on said first conductive layer;	formed on a second portion of said substrate (C)		above and in contact with a second part of the substrate	above and in contact with a second part of the substrate	Produced above, supported by, and in contact with a second portion of the substrate
a second conductive layer formed on a first portion of said first insulative layer;	formed on a first portion of said first insulative layer (C)		above and in contact with a first part of the first insulative layer	above and in contact with a first part of the first insulative layer	Produced above, supported by, and in contact with a first portion of the first insulative layer
	insulative layer (C)	A thickness of non-conductive material (such as SiNx) that has high electrical resistance. [Previously Agreed upon Construction]	a thickness of non-conductive material (such as SiNx) that has high electrical resistance.	Plain meaning	plain meaning
a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;	formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer (C)		above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer	above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer	Produced above, supported by, and in contact with the second conductive layer and a second portion of the insulative layer covering the top surface of the first conductive layer
	Overlying (C)	Above [Previously Agreed upon Construction]	above	this term should be construed as part of the larger term ("formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer"	covering the top surface of

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
an indium tin oxide layer formed on said second insulative layer,	indium tin oxide layer (C)	A thickness of indium tin oxide (ITO). [Previously Agreed upon Construction]	A thickness of indium tin oxide (ITO).	A thickness of indium tin oxide (ITO).	A thickness of indium tin oxide (ITO).
wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and	contact hole is provided through ... layer[s] (C, A)	The contact hole is formed in the layer.	the contact hole is formed in the layer	the contact hole is formed in the layer(s)	The contact hole is formed in the layers
	contact hole (C)	an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection. [Previously Agreed upon Construction]	an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.	An opening formed in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.	plain meaning
	provided through (C)	*see* construction for "contact hole is provided through . . . layer"	the contact hole is formed in the layer	Plain meaning.	see above
	expose part of said ... layer (C)		removing portions of one or more layers to uncover at least part of another layer	Plain meaning	plain meaning
	extends through (C)		is disposed in	Plain meaning	plain meaning
	electrically connect ... with (C)		provide an electrical conduction path between the first and second conductive lavers	plain meaning	plain meaning

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.	one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor (C, A)		one, but not both, of the first and second conductive layers is directly connected to one terminal of a thin film transistor	The first conductive layer is connected to the gate, source or drain of a thin film transistor, and/or the second conductive layer is connected to the gate, source or drain of the thin film transistor.	At least one of the first and second conductive layers is electrically connected to at least one of the source, drain, and gate electrodes of a thin film transistor.
	one of said first and second conductive layers (C)	The court construed "one of" as "one, but not both, of the first and second conductive layers."	one, but not both, of the first and second conductive layers	this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"	at least one of the first and second conductive layers
	one (L)		A single layer	This term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor."	plain meaning
	connected to (C, A)		directly connected to	Plain meaning	Electrically connected to
	one of a plurality of terminals of a thin film transistor (L)	One of the terminals (i.e., source, drain, or gate) of a thin film transistor. [Previously Agreed upon Construction]	one of the terminals (i.e., source, drain, or gate) of a thin film transistor	This term should be construed as part of the larger term "one of said first and second conductive layers is connected to	at least one of the source, gate and drain electrodes of a thin film transistor

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
				one of a plurality of terminals of a thin film transistor."	
	a plurality of terminals of a thin film transistor (C)		the terminals (i.e., source, drain, or gate) of a thin film transistor	this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor" to the extent that the embedded term "terminals of a thin film transistor" needs to be construed, CMO proposes the following construction: the gate, source, and drain of a thin film transistor	source, drain and gate electrodes of a thin film transistor
	thin film transistor (C)		A three terminal device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the	A three terminal semi-conductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin- film techniques on an insulating substrate rather than in a single crystal silicon wafer.	field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.
Claim 10: A liquid crystal display device comprising:	liquid crystal display device (C)	a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel. [Previously Agreed upon Construction]	a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel.	A type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel.	plain meaning
a substrate;	Substrate (C)	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support. [Previously Agreed upon Construction]	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
a first conductive layer on said substrate including: **a gate electrode,** **a gate pad, and** **a source pad;**	Conductive layer (L, C)	See Claim 1 above	See Claim 1 above	See Claim 1 above	See Claim 1 above
	gate electrode (C, A)	A patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode.	a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode	A patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode.	A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode
	gate pad (C, A)	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a gate driving circuit.	a portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit.	a patterned, electrically, conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit
	source pad (L, C, A)	A portion of the patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a data driving circuit.	a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit.	A patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit
a gate insulating film on said surface of said substrate,	a gate insulating film on said surface of said substrate (C)		a thickness of non-conductive material (such as SiNx) that has high electrical	Plain meaning	A gate insulating film above, supported by, and in contact with the surface of the substrate

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			resistance and insulates the transistor gate from the semiconductor above and in contact with at least part of the surface of the substrate		
	gate insulating film (C)		a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor	Plain meaning	Plain meaning; or Insulating film formed over the gate region
	insulating film (C)	A thickness of non-conductive material (such as SiNx) that has high electrical resistance. [Previously Agreed upon Construction]	a thickness of non-conductive material (such as SiNx) that has high electrical resistance		plain meaning
a portion of said gate insulating film overlying said gate electrode;					
a semiconductor layer on said portion of said gate insulating film;	a semiconductor layer on said portion of said gate insulating film (C)		a thickness of semiconductor material above and in contact with a part of the gate insulating film	a thickness of semiconductor material above and in contact with a part of the gate insulating film	A semiconductor above, supported by, and in contact with the portion of the gate insulating film.
	semiconductor layer (C)	A thickness of a semiconductor material, such as amorphous silicon. [Previously Agreed upon Construction]	a thickness of semiconductor material, such as amorphous silicon	A thickness of a semiconductor material, such as amorphous silicon	plain meaning
an impurity-doped	impurity-doped	A thickness of	a thickness of	A thickness of	Plain meaning;

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
semiconductor layer on said semiconductor layer;	semiconductor layer (C)	semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity. [Previously Agreed upon Construction]	semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity	semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity.	or Semiconductor layer doped with impurities
a source electrode and a drain electrode on said semiconductor layer;	a source electrode and a drain electrode on said semiconductor layer (A)		a source electrode and a drain electrode above and in contact with the semiconductor layer	a source electrode and a drain electrode above and in contact with the semiconductor layer	The source electrode and the drain electrode above, supported by, and in contact with the semiconductor layer
	source electrode (C, A)	A patterned, electrically conductive material formed over the source region, current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	Construe term: "a source electrode and a drain electrode" as: Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and the drain electrode of the transistor under control of the gate electrode of the	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
				transistor.	
	drain electrode (C, A)	A patterned, electrically conductive material formed over the drain region, current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode.	this term should be construed as part of the larger term "a source electrode and a drain electrode" (see above)	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;	passivation layer (C)	A thickness of insulative material that provides protection such as electrical stability and chemical isolation. [Previously Agreed upon Construction]	a thickness of insulative material that provides protection such as electrical stability and chemical isolation	A thickness of insulative material that provides protection such as electrical stability and chemical isolation.	plain meaning
a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad; **a second contact hole provided through said passivation layer exposing said drain electrode;**					
a third contact hole provided through said passivation layer and said gate insulating film exposing said gate	exposing said gate pad portion (A)		removing portions of one or more layers to uncover at least part of a gate pad [portion]	Plain meaning	Causing the gate pad to be exposed to the atmosphere
	exposing (C)		removing portions of	Plain meaning	Laying open or causing to

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
pad;			one or more layers to uncover at least part of another layer		be exposed from above
a fourth contact hole provided through said passivation layer exposing said source electrode;					
a pixel electrode electrically connected with said drain electrode via said second contact hole; and	pixel electrode (C)	a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device. [Previously Agreed upon Construction]	a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device	electrode controlling the brightness of a pixel	Electrode controlling the brightness of a pixel
a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.	transparent conductive layer (C)	A thickness of transparent electrically conductive material. [Previously Agreed upon Construction]	a thickness of transparent electrically conductive material	Plain meaning	plain meaning
	electrically connecting (A)		provide an electrical conduction path	Plain meaning	plain meaning
Claim 11: A method of manufacturing a liquid crystal display device, comprising the steps of:	a method of manufacturing a liquid crystal display device (C)		a process for producing a liquid crystal display device	Plain meaning	plain meaning

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
forming a first conductive layer on a substrate;	Substrate (C)	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support. Previously Agreed upon Construction]	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
	Conductive layer (L, C)	See Claim 1 above	See Claim 1 above	See Claim 1 above	See Claim 1 above
patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;					
forming an insulating film on said substrate including said patterned conductive layer;					
forming a semiconductor layer on said insulating film;					
forming an impurity-doped semiconductor layer on said semiconductor layer;					
patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;	patterning ... to form an active layer (C)		the removal of selected portions of the impurity-doped semiconductor layer and the semiconductor layer using etching techniques in order to	Plain meaning	selectively removing portions of ... using etching techniques in order to form an active region

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
			form an active layer		
	patterning (C)	the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material [Previously Agreed upon Construction]	the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material	Plain meaning	selectively removing portions of a surface using etching techniques in order to produce a pattern in the remaining material
	active layer (C, A)	A discrete portion of the semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode.	a discrete portion of semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode.	A discrete portion of the semiconductor layer that is formed by patterning and located along the gate electrode of a thin film transistor. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode of the thin film transistor.	active region of a thin film transistor
forming a second conductive layer overlying said substrate including said active layer;					
patterning said second conductive layer to form source electrode and a drain electrode on said active layer;					

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;					
selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;	selectively etching (C)		The removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.	Plain meaning	selectively removing portions of a surface using etching techniques in order to produce a desired pattern in the remaining material
patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;	patterning a pixel electrode electrically connected to said drain electrode (C)		the removal of selected portions of a pattern of transparent electrically conductive material to form a pixel electrode that has an electrical conduction path with the drain electrode	Plain meaning	selectively removing portions of a pixel electrode using etching techniques in order to electrically connect the pixel electrode to the drain electrode
	electrically connected (A)		provide an electrical conduction path	Plain meaning	plain meaning
patterning a first	electrically connected (A)		provide an electrical	Plain meaning	plain meaning

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court or Agreed Upon Construction	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
transparent conductive layer electrically connected to said gate pad through said third contact hole; and			conduction path		
patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.	electrically connecting (A)		provide an electrical conduction path	Plain meaning	plain meaning

	U.S. Patent No. 6,664,569 Terms & Limitations	LGD's Proposed Construction	AUO's Proposed Construction
Claim 17: A liquid crystal display (LCD) device, comprising:			
a substrate;			
a gate line on the substrate and extending along a first direction, the gate line having an opening therein; a first insulating layer on the gate line;	the gate line having an opening therein (A)	the gate line has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment	Gate line with a cut out extending from the periphery of the gate line to the interior of the gate line
	a gate line (L)	a pattern of electrically conductive material that conveys gate signals to transistors, a portion of which controls current flow through the channel between the source and drain electrodes	An elongated directional conductor that supplies signals to gate electrodes
	having an opening therein (L)	has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment	Having a cut out extending from the periphery to a point within
a semiconductor layer on the first insulating layer over at least a portion of the opening; a data line on the insulating layer and extending along a second direction substantially perpendicular to the first direction;	a semiconductor layer on the first insulating layer over at least a portion of the opening (A)	a layer of semiconductor material, above and supported by or in contact with the first insulating layer, a portion of which overlaps art of the space in the gate line	A semiconductor layer above, supported by, and in contact with the first insulating layer, the semiconductor layer being over at least a portion of the opening in the gate line
a drain electrode on the semiconductor layer over at least a portion of the opening; and	a drain electrode on the semiconductor layer over at least a portion of the opening (A)	a drain electrode, above and supported by or in contact with the semiconductor layer, a portion of which overlaps part of the space in the gate line	A drain electrode above, supported by, and in contact with the semiconductor layer, the drain electrode being over at least a portion of the opening in the gate line
	drain electrode (A)	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of

	U.S. Patent No. 6,664,569 Terms & Limitations	LGD's Proposed Construction	AUO's Proposed Construction
		electrode under control of the gate electrode.	the gate electrode.
a source electrode on the semiconductor layer, extending from the data line and being separated and spaced apart from the drain electrode.			
Claim 19: The LCD device to claim 18, further comprising a pixel electrode disposed in a pixel region that is defined by an intersection of the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.	pixel electrode (A)	a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device	Electrode controlling the brightness of a pixel
Claim 21: The LCD device of claim 17, wherein the source electrode substantially surrounds the drain electrode.	substantially surrounds the drain electrode (A)	extending considerably around a portion of the drain electrode	Surrounds almost all the drain electrode portion
	Substantially (A)	considerably	Almost all
Claim 25: A liquid crystal display (LCD) device, comprising:			
a substrate;			
a gate line on the substrate and extending along a first direction, the gate line including a gate electrode, the gate electrode having an opening therein, wherein the opening includes a first opening portion and a second opening portion;	the gate electrode having an opening therein (A)	the gate electrode has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain laver misalignment	gate electrode with a cut out extending from the periphery of the gate line to the interior of the gate line
	gate electrode (L, A)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
	the opening includes a first	the space in the gate electrode pattern	Non-rectangular-shaped opening having two

	U.S. Patent No. 6,664,569 Terms & Limitations	LGD's Proposed Construction	AUO's Proposed Construction
	opening portion and a second opening portion (A)	includes a first part to primarily compensate for gate-drain layer misalignment and a second part to primarily reduce gate-drain capacitance	distinct opening portions
	a first opening portion (L)	a first part to primarily compensate for gate-drain layer misalignment	One distinct opening portion
	a second opening portion (L)	a second part to primarily reduce gate-drain capacitance	Another distinct opening portion
a first insulating layer on the gate line;			
a semiconductor layer on the first insulating layer;			
a data line on the insulating layer and extending along a second direction;			
a drain electrode having a first electrode and a second electrode, the first electrode of the drain electrode overlapping at least a part of the first opening portion of the gate electrode; and	a first electrode (L)	a first portion of the drain electrode to primarily compensate for gate- drain layer misalignment	One distinct portion of a single electrode
	a second electrode (L)	a second portion of the drain electrode to primarily reduce gate-drain capacitance	Another distinct portion of a single electrode
a source electrode on the semiconductor layer, extending from the data line and being separated and spaced apart from the drain electrode.	source electrode (A)	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
Claim 32: The liquid crystal display device of claim 25, further comprising a pixel electrode and the drain	a third electrode (L)	a third portion of the drain electrode to primarily connect to the pixel electrode	The third distinct portion of the single electrode

	U.S. Patent No. 6,664,569 Terms & Limitations	LGD's Proposed Construction	AUO's Proposed Construction
electrode further comprising a third electrode contacting the pixel electrode.			
Claim 34: The liquid crystal display device of claim 32, wherein the second electrode of the drain electrode connects the first and third electrodes of the drain electrodes.	Connects (L)	joins	physically attached

	U.S. Patent No. 6,803,984 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1: A method for manufacturing a liquid crystal display device, comprising the steps of:				
providing at least a first substrate and a second substrate on a single production process line;	a first substrate (C)	one of a TFT or color filter substrate	Plain meaning	Plain meaning; Or one of the two opposing substrates of the liquid crystal cell
	a second substrate (C)	the other of the TFT or color filter substrate	The substrate immediately following the first substrate	Plain meaning Or the other of the two opposing substrates of the liquid crystal cell
	on a single production process line (L)	on a production line where the processing equipment is arranged along a common path for performing the liquid crystal cell processes	On a line structure for processing the substrates in only one direction without branching	On a production line for processing liquid crystal displays in a single, linear arrangement

	U.S. Patent No. 6,803,984 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
passing the first and second substrates through a sealing material coating portion of the single production process line in serial order,	passing the first and second substrates through a sealing material coating portion of the single production process line in serial order (C)	passing the first and second substrates, one after the other, along a portion of the single production process line where the sealing material is selectively applied	Providing the first and second substrates, one after the other without anything in between, in at one end, of a machine for coating sealing material in the single production process line in which the same order of the first and second substrates is maintained throughout the seal dispensing process	providing the first and second substrates one after the other, without anything in between; in at one end, and out at the other end in the same order of an equipment/machine[1] for coating sealing material on a substrate
	a sealing material coating portion of the single production process line (A)	a portion of the single production process line where the sealing material is selectively applied	a machine for coating sealing material in the single production process line	An equipment/machine for coating sealing material in the single production process line.
	in serial order (A)	one after the other	one after the other one without anything in between	One after the other without anything in between
a sealing material being coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon;				
passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order, liquid crystal	passing the first and second substrates through a liquid crystal dispensing portion of the single production process line in serial order (C)	passing the first and second substrates, one after the other, along a portion of the single production process line where liquid crystal is selectively dispensed	providing the first and second substrates, one after the other without anything in between, in at one end, and out at the other end, of a machine for dispensing liquid crystal material in the	providing the first and second substrate one after the other, without anything in between; in at one end, and out at the other end in the same order of the liquid crystal dispensing

[1] Due to a clerical error, the word "equipment" as inadvertently omitted from the previously submitted JCC. It is reinserted herein.

	U.S. Patent No. 6,803,984 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
being dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon; and			single production process line in which the same order of the first and second substrates is maintained throughout the liquid crystal dispensing process	machine/equipment
	a liquid crystal dispensing portion of the single production process line (A)	a portion of the single production process line where liquid crystal is selectively dispensed	a machine for dispensing liquid crystal in the single production process line	an equipment/machine for dispensing liquid crystal on a substrate in the single production process line
	a pixel region (C)	area corresponding to the inside of the sealing material	an area with pixels	Area with pixel
assembling the first substrate with the second substrate to form a liquid crystal panel of at least one liquid crystal display device.	assembling (C)	bring together	Indefinite	Indefinite
Claim 5: The method according to claim 4, wherein the first substrate is disposed in the liquid crystal dispensing portion and the liquid crystal is dispensed onto the first substrate at the same time that the second substrate is disposed in the sealing material coating portion.	the liquid crystal is dispensed onto the first substrate at the same time that the second substrate is disposed in the sealing material coating portion (A)	a point in time when liquid crystal is being dispensed on the first substrate overlaps with a point in time when the second substrate is located in the portion of the single production process line where the sealing material is selectively applied	when the liquid crystal is dispensed onto the first substrate in the machine for dispensing liquid crystal, the second substrate is located in the machine for coating sealing material	when the liquid crystal is dispensed onto the first substrate in the liquid crystal dispensing machine, the second substrate is located in the sealant coating machine
Claim 10: The method according to claim 1, further comprising the step of cleaning the first	in serial order in a same cleaning unit (L)	one after the other in the same cleaning equipment	one after the other without anything in between, in a same cleaning machine	cleaning the first substrate and the second substrate one after the other without anything in between in the same cleaning

	U.S. Patent No. 6,803,984 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
substrate and the second substrate in serial order in a same cleaning unit.				machine

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1: A thin film transistor comprising:	transistor (C)	a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate	a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate electrode, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate	Plain meaning Or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.[2]
a substrate; and	substrate (C)	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
a gate including a	gate (L)	patterned electrically conductive	A region of a transistor.	same as gate electrode; a

[2] The phrase "rather than a single crystal silicon wafer" was inadvertently omitted from the previously submitted JCC due to a clerical error. It is reinserted herein.

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm.		material that includes a portion that controls current flow through the channel between the source electrode and drain electrode		patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
	a double-layered structure (C, A)	a structure of an electrically conductive material that includes two sequentially deposited metal layers	A structure having only two metal layers.	a two-layered step structure
	a second metal layer disposed on the first metal layer (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is in contact with the first metal layer.	a second metal layer precipitated above, supported by and in contact with the first metal layer
	the first metal layer including aluminum (C)	the first metal layer containing aluminum and possibly other materials	plain meaning	plain meaning
	the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer (C)	the second metal layer is patterned to prevent hillock on the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer	The second metal layer prevents hillock on the sides of the aluminum first metal layer.	the second metal layer being arranged on the first metal layer to prevent hillocks from forming on the side portions of the aluminum first metal layer
	at the sides of the aluminum first metal layer (L, C, A)	the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer	Indefinite.	at the portions on the top surface of the first metal layer not covered by the second metal layer
	the first metal layer being wider than the second metal layer by about 1 to 4 μm (L, C, A)	the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together	The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the	Indefinite; or

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
		with the portions exposed to the subsequently deposited gate insulating layer, is more than 1μm and less than 4μm greater than the width of the second metal layer	second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.	the first metal layer is about 1 to 4 μm greater than the width of the second metal layer measured from a level defined by the top of the first metal layer
Claim 2: The thin-film transistor as claimed in claim 1, wherein the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second metal layer disposed thereon have the same width as each other.	two side portions of the first metal layer having no second layer disposed thereon (C, A)	the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	the two side portions on the top surface of the first metal layer not covered by the second layer
Claim 4: A thin film transistor comprising:	transistor (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
a substrate;	substrate (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first	gate (L)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	a double-layered structure (C, A)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	A second metal layer disposed on the first metal layer (L, C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	the first metal layer including aluminum (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the	See Claim 1 above	See Claim 1 above	See Claim 1 above

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm;	aluminum first metal layer (C)			
	at the sides of the aluminum first metal layer (L, C, A)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	the first metal layer being wider than the second metal layer by about 1 to 4 μm (L, C, A)	See Claim 1 above	See Claim 1 above	See Claim 1 above

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
a first insulating layer disposed on the substrate including the gate;				
a semiconductor layer disposed on a portion of the first insulating layer at a location corresponding to the gate;				
an ohmic contact layer disposed on two sides of the semiconductor layer;				
a source electrode and a drain electrode disposed on the ohmic contact layer and extending onto the first insulating layer; and				
a second insulating layer covering the semiconductor layer, the source and drain electrodes and the first insulating layer.				
Claim 5: The thin-film transistor as claimed in claim 1, wherein the second metal layer is located in a middle portion of the first metal layer so that two side	two side portions of the first metal layer having no second layer thereon (C)	the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	The two side portions on the top surface of the first metal layer not covered by the second layer

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
portions of the first metal layer having no second metal layer disposed thereon have the same width as each other.				

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 7: A method of forming a thin film transistor comprising:	transistor (C)	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate	Plain meaning Or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.[3]
forming a first metal layer on a substrate,	substrate (C)	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	plain meaning
forming a second metal layer on the first metal	forming a second metal layer on the first metal	sequentially depositing the second metal layer above and in contact with	The second metal layer is formed in direct contact	forming a second metal layer above, supported by, and in

[3] The phrase "rather than a single crystal silicon wafer" was inadvertently omitted from the previously submitted JCC due to a clerical error. It is reinserted herein.

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
layer;	layer (L, C)	the first metal layer	with the first metal layer.	contact with the first metal layer
simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.	a double-layered metal gate (C, A)	a patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode	A double-layered metal gate is a gate having only two metal layers.	a gate electrode having a two-layered step structure
	gate (L)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A region of a transistor.	same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
	a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm (L, C, A)	the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4μm greater than the width of the second metal layer	The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.	Indefinite; or the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer
Claim 7: A method of forming a thin film transistor comprising: forming a first metal layer on a substrate, forming a second metal	simultaneously patterning (A)	removing part of the first and second metal layers during a single etching process	Plain meaning	Forming the patterned first and second metal layers at the same time in one chemical etching step

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
layer on the first metal layer; simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.				
Claim 8: The method of claim 7, wherein the first and second metal layers are patterned so that the first metal layer has a first and a second side portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.	a first and a second side portion being exposed from the second metal layer (C)	first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	A first side portion and a second side portion on the top surface of the first metal layer not covered by the second layer
Claim 10: The method of claim 7, wherein the patterning step is such that the second metal layer is etched faster than the first etching layer.	first etching layer (L)	the first metal layer	Indefinite.	Indefinite
Claim 16: A method of waking a thin-film transistor, comprising the steps of:	transistor (C)	See Claim 7 above	See Claim 7 above	See Claim 7 above
	Waking (L)	making	Indefinite.	non-sensical; indefinite

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
depositing a first metal layer on a substrate, the first metal layer including aluminum;	the first metal layer including aluminum (C)	the first metal layer containing aluminum and possibly other materials	A first metal layer that includes pure aluminum.	plain meaning
depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;	depositing a second metal layer on the first metal layer (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is deposited in direct contact with the first metal layer.	Precipitating a second metal layer above, supported by, and in contact with the first metal layer
forming a single photoresist having predetermined width on the second metal layer;	forming a single photoresist having a predetermined width on the second metal layer (C)	forming a pattern of single photosensitive material that has a specified width on the second metal layer	The photoresist is deposited in direct contact with the second metal layer.	plain meaning
	Photoresist (C)	pattern of a photosensitive material	An etching mask.	plain meaning
patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and removing the photoresist.	simultaneously in a single etching step using the single photoresist as a mask (L)	during a single etching process with a common mask	The first and second metal layers are simultaneously etched in a single step using the photoresist as a mask.	Construe term: "patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask" as forming the patterned first and second metal layers in one chemical etching step using one photoresist mask

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
	patterning ... simultaneously (A)	Removing part of the first and second metal layers during a single etching process	Plain meaning	forming the patterned first and second metal layers in one chemical etching step
	the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm (L, C, A)	the first and second metal layers are etched such that the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4μm greater than the width of the second metal layer	The first metal layer being etched so that a top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.	indefinite; or the first metal layers being etched so that the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer
Claim 22: The method of making a thin film transistor as claimed in claim 16, wherein two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other.	two side portions of the first metal layer having no second metal layer deposited thereon (C, A)	the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning.	The two portions on the top surface of the first metal layer not covered by the second metal layer

	U.S. Patent No. 7,176,489 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1. A thin film transistor comprising:	transistor (C)	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate	Plain meaning Or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.[4]
a substrate; and	Substrate (C)	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	Plain meaning; Or The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.

[4] The phrase "rather than a single crystal silicon wafer" was inadvertently omitted from the previously submitted JCC due to a clerical error. It is reinserted herein.

	U.S. Patent No. 7,176,489 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
a double-layered metal gate having a first metal layer and a second metal layer thereon, a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm.	a double-layered metal gate (C, A)	[a] patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode	A gate having only two metal layers.	A gate electrode having a two-layered step structure
	gate (L)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A region of a transistor.	same as gate electrode; a patterned electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode
	having a first metal layer and a second metal layer thereon (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is in contact with the first metal layer.	The double layered metal gate having a first metal layer and a second metal layer formed on the top surface of the first metal layer
	a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm (L, C, A)	the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4μm greater than the width of the second metal layer	The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a gate where not all of the top surface of the first metal layer is covered by the second metal layer.	Indefinite; or The width of the first metal layer is about 1 to 4 μm greater than the width of the second metal measured from a level defined by the top of the first metal layer
Claim 2. The transistor of claim 1, wherein the first metal layer has a first and second side	a first and second side portion being exposed from the second metal layer (C, A)	first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	The two side portions on the top surface of the first metal layer not covered by the second metal layer

	U.S. Patent No. 7,176,489 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.				
Claim 3. The transistor of claim 2, wherein each side portion of the first metal layer is less than about 2 μm in width.	side portion of the first metal layer (A)	side surface of the first metal layer exposed to the subsequently deposited gate insulating layer	Plain meaning	*Construed with "each" in front:* Each of the first and second side portions on the top surface of the first metal layer not covered by the second metal layer

	U.S. Patent No. 7,218,374 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
Claim 1: A method of manufacturing a liquid crystal display (LCD) device comprising:				
preparing a lower substrate and an upper substrate;	preparing a lower substrate and an upper substrate (C)	making the substrates ready for depositing sealant and liquid crystal material prior to attachment	indefinite	indefinite
forming an auxiliary sealant and subsequently forming a main sealant on one of the lower and upper substrates, wherein the auxiliary sealant is formed in a dummy region and connects to the main sealant, and wherein the auxiliary sealant and the main sealant are contiguous;	forming a main sealant (L)	depositing sealant material that encloses the display region	Forming sealing material necessary for confining liquid crystal from leaking out from between the substrates.	forming a segment of sealant that encloses the liquid crystal in the LCD panel
	main sealant (C, A)	sealant material that encloses the display region	sealant material necessary for confining liquid crystal from leaking out from between the substrates	a segment of sealant for enclosing the liquid crystal in the LCD panel
	auxiliary sealant (C, A)	sealant deposited in an area outside of the main sealant	sealant material that is not necessary for confining liquid crystal from leaking out from between the substrates	A segment of sealant that extends from the main sealant and is outside the enclosure of the main sealant
	a dummy region (L, A)	an area outside of the main sealant	an area outside the boundary of the main sealant	An area outside the enclosure of the main sealant
	connects to the main sealant (L)	joined to the main sealant	physically attached to the main sealant	Physically attached to the main sealant
	wherein the auxiliary sealant and the main sealant are contiguous (L, C, A)	wherein the auxiliary and main sealants are deposited in a continuous process	wherein the auxiliary sealant touches but does not overlap the main sealant	Wherein the auxiliary sealant and the main sealant are physically connected to each other

	U.S. Patent No. 7,218,374 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
applying a liquid crystal on one of the lower and upper substrates;	applying a liquid crystal on one of the lower and upper substrates (L, C, A)	depositing the liquid crystal onto either one of the substrates	Plain meaning.	plain meaning
attaching the lower and upper substrates; and	attaching the lower and upper substrates (A)	pressing the lower and upper substrates together	putting the lower and upper substrates together as one single piece	Putting the lower and upper substrates together as one single piece
curing at least the main sealant.				
Claim 2: The method of claim 1, wherein the main sealant and the auxiliary sealant are at least partially curable by irradiating UV light and curing the main sealant includes irradiating UV light.				
Claim 5: The method of claim 2, wherein the sealant is formed using oligomers each having one end coupled to an acrylic group and the other end coupled to an epoxy group.				
Claim 10: The method of claim 2, wherein a region where the sealant is not formed is covered with a mask during the irradiating with UV light.				
Claim 11: The method of claim 2, wherein a region				

	U.S. Patent No. 7,218,374 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
where the main UV sealant is not formed is covered with a mask during the irradiating with UV light.				
Claim 16: The method of claim 1, further comprising cutting the attached substrates.				
Claim 17: The method of claim 16, wherein the attached substrates are cut across a portion of the auxiliary sealant.				
Claim 21: A method of manufacturing a liquid crystal display (LCD) device comprising:				
preparing a lower substrate and an upper substrate;				
forming an auxiliary UV sealant and a main UV sealant on one of the lower and upper substrates, wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant, wherein the auxiliary UV sealant contacts the main UV sealant;	forming a main UV sealant (L)	The combination of the construction for "forming a main sealant" with the agreed construction of "UV sealant"		
	main UV sealant (C, A)	The combination of the construction for "main sealant" with the agreed construction of "UV sealant"		
	UV sealant (C)	sealant material that is at least partially curable by UV light	sealant material that is at least partially curable by UV light	sealant material that is at least partially curable by UV light
	wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant (L, C, A)	wherein the auxiliary UV sealant is deposited in an area that is outside of the main UV sealant and is joined to the main UV sealant	Wherein the auxiliary UV sealant is formed in an area outside the boundary of the main UV sealant beginning from the main UV sealant and moving outward	Wherein the auxiliary UV sealant is formed in an area outside the enclosure of the main UV sealant

	U.S. Patent No. 7,218,374 Terms & Limitations	LGD's Proposed Construction	CMO's Proposed Construction	AUO's Proposed Construction
	auxiliary UV sealant (C, A)	UV sealant deposited in an area outside of the main UV sealant		a segment of UV sealant that extends from the main sealant but not used to enclose liquid crystal in the finished LCD panel
	wherein the auxiliary UV sealant contacts the main UV sealant (C, A)	wherein the auxiliary UV sealant touches the main UV sealant	wherein the auxiliary UV sealant touches the main UV sealant.	wherein the auxiliary sealant and the main sealant are physically connected together
applying a liquid crystal on one of the lower and upper substrates;				
attaching the lower and upper substrates; and				
irradiating UV light on the attached substrates.				